Additively Manufactured Photovoltaic Inverter (AMPVI)

Prime: National Renewable Energy Laboratory

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Project Objective

- To enable integration of hundreds of GWs of solar generation to the U.S. electric power system, this project will develop a unique PV inverter design that combines high-voltage Silicon Carbide (SiC) with revolutionary concepts such as additive manufacturing and multi-objective magnetic design optimization.

- The final deliverables from the project will include:
  a) High power density (>100W/in\(^3\)), high efficiency (>98%) power block and 50 kW prototype inverter
  b) Additive manufacturing techniques for power block and heat sink
  c) Magnetic design optimization tool
  d) A versatile controller
  e) Standard HIL inverter testing techniques
  f) Cost and reliability analysis of SiC based PV inverter
### Power Electronics Target Metrics

| Attribute                                      | Target Metric
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Conversion Efficiency: Defined as the ratio of the usable output power (AC or DC) versus available input power from the PV panels. Typically, the PV inverters in the U.S. are tested to the CEC (California Energy Commission) efficiency using a weighted formula(^\text{19})</td>
<td>&gt; 98%</td>
</tr>
<tr>
<td>Service Life and Reliability: Defined as the useful life of the power electronic subsystems to support the required plant availability under normal operation and maintenance</td>
<td>&gt; 25 years(^\text{20})</td>
</tr>
<tr>
<td>Power Density: Defined as the ratio of rated output power versus device volume and weight.</td>
<td>&gt; 100 W/in(^3) for residential and small commercial systems</td>
</tr>
<tr>
<td>System Cost: Defined as the lifetime cost of the power electronic device, including initial capital cost and the operation and maintenance (O&amp;M) cost over the service life.</td>
<td>&lt; $0.10/W, utility scale &lt; $0.125/W, commercial scale &lt; $0.15/W, residential scale</td>
</tr>
<tr>
<td>Grid-Support Functions: These include a host of smart inverter functions such as volt/var, volt/watt, frequency/watt, voltage ride-through, power factor control, reactive power support, ramp rate control, and so on. These functions can be activated either autonomously through default settings or remotely through utility SCADA commands.</td>
<td>Compliance with ANSI, IEEE, and NERC standards(^\text{21,22,23})</td>
</tr>
<tr>
<td>Interoperability: Defined as the capability of the power electronic devices to exchange and readily use information—securely, effectively with other system components.</td>
<td>Compliance with Open Standards which include SunSpec Modbus, Smart Energy Profile (SEP 2), IEC 61850, MultiSpeak, and DNP3</td>
</tr>
</tbody>
</table>

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SunShot PE Target Metrics

SunShot

U.S. Department of Energy
Project Technical Approach

AMPVI

- Power Density > 100W/in³
- η > 98%
- Life > 25 yrs.
- Interoperable
- Cost < $0.125/W

Superior Switches
1700 V SiC MOSFET
Novel Packaging
Superior Packaging

Power Block Architecture
Additive Manufacturing
Flexible Control & Comm.
Economies of Scale

Multi-objective Optimization
Mother & Daughterboard
Optimized Magnetics
Flexible Control & Comm.

Holistic Approach
System Validation
PHIL Testing

Current State

High Cost
Discrete Components
Manuf. Specific Controller
Generic Magnetics

Low Voltage Design
Low Reliability
Not Interoperable

Tough SiC Packaging
Low Cost
Low Reliable
Project Technical Approach

**Topology**
- Communications
  - Digital Controller (Optional to Power Block)
  - Auxiliary Power
  - Gate Driver
  - Protection
  - Measurements
  - AC Side
  - DC Side
- Film Cap
- SIC Power Poles
- Air In
- Integrated Heat Sink
- Air Out

**Controller**
- Motherboard
- Stacked Daughterboards

**AM-based Power Block**
- Busbars, Lead frame
- DC-bus capacitors
- Controller PCB
- Gate driver PCB
- Sensors
- Power modules
- Heatsink

**Magnetic Design**
- Solid Body Analysis
- Change Geometry
- Change Parameter
- RLC EM
- Program and Data Flow
- Control
- Temperatures

**Thermal and Mechanical Design**
- Power Block Assembly
- Control Board Assembly
- Front View
- Side View
- LCL Filter - L
- LCL Filter - C
- LCL Filter - C [0.059 Liter(L)]

**System-level Validation**
- Inverter Current Measurements
- AC Grid Simulator
- PV Simulator or DC Source
- AMPV1
- Real-time Simulator
- Voltage Commands
- Reduced-order Distribution Model

**Electrical Circuit Analysis**
- Reduced Order Distribution Model

**Thermal Analysis**
- Program and Data Flow
- Control
- Temperatures

**Program and Data Flow**
- Reduced Order Distribution Model
- PV Simulator or DC Source
- AMPV1
- AC Grid Simulator
- Real-time Simulator
- Voltage Commands
## Economies of Scale

<table>
<thead>
<tr>
<th>DG Source</th>
<th>Source Converter (Power Block 1)</th>
<th>Grid Converter (Power Block 2)</th>
<th>Utility</th>
</tr>
</thead>
<tbody>
<tr>
<td>PV, Fuel Cell</td>
<td>![Diagram 1]</td>
<td>![Diagram 2]</td>
<td>Single Phase</td>
</tr>
<tr>
<td>Wind, Microturbine, IC Engine, Flywheel</td>
<td>![Diagram 3]</td>
<td>![Diagram 4]</td>
<td>Three Phase</td>
</tr>
<tr>
<td>Battery</td>
<td>![Diagram 5]</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

* Non-operational

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AM-based Power Block with 1700V SiC MOSFETs and Diodes

Dynamic Characterization of SiC MOSFET

Power Block Assembly

Switch Package

Phase-leg Module with Cooling System

Fabricated All-SiC Module

Gate Driver Board

3D Printed Heatsink

Thermal Analysis

Phase-leg Module with Cooling System and DC Capacitors

Three-phase Power Block

Switch Package
The switching performance of the SiC module is evaluated through a high voltage double pulse test setup.

- Power stage with high voltage (>2000V DC) and current capability (>20A RMS)
- Embedded solid-state circuit breaker for fast and reliable overcurrent protection
- Preliminary test: 700V dc bus voltage and 55A load current
- Excellent turn-on switching behavior; moderate turn-off ringing due to non-optimized external power loop connection
Inductor Design Using Multi-Objective Optimization

AMPVI Circuit Topology

Multi-Objective Design Methodology

Evolutionary Computing for MO Design
Example: AC Inductor Design

Integrated Analysis
Magnetic – MEC
Thermal – TEC

Losses
AC resistive losses (skin effect)
Proximity effect loss
Core loss (hysteresis + eddy)

Constraints
Geometry/bending radius
Aspect ratio
Mass/Loss
Current density
Inductance (and variation)
Cross-inductance
Peak wind. temperature

Objectives (minimize)
Volume
Loss

Inverter Side Current

Pareto-Optimal Front

Y-Core AC Inductor
Top View
Profile View
Controller

Control Algorithms and Simulation Validation

Grid-tied Current Control

4-Quadrant Operation

Advanced Functions
(VVAR, FWATT, Ride through, AI etc.)

Controller Hardware and Interface

Power Module

ORNL Gate Driver Board

Interface Board

SBRIO: Xilinx Zynq-7000, 667 MHz dual-core ARM Cortex-A9 processor, an Artix-7 FPGA, and a mezzanine card connector
Controller Hardware-in-the-Loop (CHIL)

CHIL Experimental Setup
- SBRI0 GUI
- Controller (SBRI0+GPIC)
- Scope
- Real time simulator
- Real time simulator GUI

Pure Simulation

CHIL System Architecture
- SBRI0 real time layer
- Advanced inverter functions
- Current command
- Feedbacks
  - V, I, f
  - Alarms
  - CB Status
- SBRI0 FPGA layer
- PWM signals
- Feedbacks
- PWM, trip signals
- Real time simulator
- Inverter model
- Feedbacks
  - Instantaneous V, I

CHIL Results
Components are grouped into three thermal subsystems:

I: DC capacitors, DC current and voltage sensors
II: power block, LCL filters
III: Control board, AC current and voltage sensors

Subsystem II has largest heat loads and therefore becomes the main focus in thermal design.

The inverter designed volume is 1378 in\(^3\), yielding a power density of approximately 36 W/in\(^3\)
Evaluation of Thermal Design

- Heat exchanger is modeled as a porous media within ANSYS
- Parameters are defined to match the desired pressure drop versus flow of the specified heat exchanger

Air Temperature Distribution

Sample Mesh

Preliminary CFD Simulations

Boundary Conditions

Velocity Vectors

Center Plane Temperature
AMPVI Design Process Flow

AMPVI

- Power Hardware
  - Magnetics
    - Common Mode Filter
    - AC Filter Design
    - Testing & Validation
  - Power Block
    - Switch Package and Power Module
    - Testing & Validation
  - Controller
    - Control Algorithm
    - Control Hardware
    - CHIL Validation

Harmonics, Losses, P, V, I, PD
Harmonics, η, PD, P, V, I
Grid support functions, Interoperable, PD

Inverter Design
- Verification
- Inverter Validation
  - Power Testing
  - System PHIL Validation (in BP 3)

Validation feedback

η, P, Harmonics, PD

ΔI_{dc} 

f_s

f_s

Thermal limits, Mechanical data

Thermal limits, Mechanical data

Thermal limits, Mechanical data

η, PD, Operational limit

System level design inputs
Inter-subsystem dependency
Subsystem design steps
System validation feedback to sub-systems

Testing & Validation

Harmonics, η, P, Harmonics, PD

Common
Mode Filter

AC Filter Design

Testing & Validation

Switch Package and Power Module

Testing & Validation

Control Algorithm

Control Hardware

CHIL Validation

System level design inputs
Inter-subsystem dependency
Subsystem design steps
System validation feedback to sub-systems
Stakeholder Engagement

- **Technology advisory panel (TAP)**
  - Getting industry feedback and building industry interest in developed technologies for future commercialization
  - TAP was formed and currently have four members Solectria, Unified Power, National Instruments, Semikron USA
    - 1-hour call in every 3 months
    - No travel requirement
    - Typically be at high level without discussing any detailed technology or IPs
    - May need to sign a multi-party NDA if detailed technologies discussed
Acknowledgements

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- We gratefully acknowledge the support of Dr. Guohui Yuan and his SunShot Systems Integration team for funding this work.

- And this workshop.

Thank You!!