### Overview

#### Timeline

- **Start** – FY13
- **Finish** – FY15
- **22% complete**

#### Barriers

- Automotive inverters designs with silicon (Si) will likely not meet the DOE APEEM 2020 targets: **Cost**, **Efficiency** and **Density** to be met.
- State-of-the-Art module packaging technologies have limitations in electrical, thermal, and thermo-mechanical performance, as well as manufacturability.

#### Targets Addressed

- 40% cost reduction and 60% power density increase of the power module, to meet the DOE power electronics 2020 targets

#### Partners

- **ORN aisle Members:** Puqi Ning, Andy Wereszczak, Laura Marlino
- **The University of Tennessee:** Fred Wang

#### Budget

- Total project funding
  - DOE share – 100%
- Funding for FY13: $700K
Project Objective

• Overall Objective

➢ Develop advanced power electronics packaging technologies for wide bandgap (WBG) inverter: Advancing automotive power modules and power inverters and converters in electrical performance, cooling capability, thermo-mechanical performance, and manufacturability, resulting in comprehensive improvement in cost-effectiveness, efficiency, reliability and power density of electric drive systems.

➢ Provide packaging support for other VT APEEM projects for systemic research: Fabrication of customer-specific power modules.

• FY13 Specific Objective

➢ Develop a set of packaging technologies and manufacture an all-silicon carbide (SiC) power module (phase leg, 100A/1200V rated) with lower thermal resistance, small electric parameters, enabling exploitation of WBG superior attributes.

➢ Deliver WBG power modules to ORNL APEEM team for improvements in cost, efficiency and density
## Milestones

<table>
<thead>
<tr>
<th>Date</th>
<th>Milestones and Go/No-Go Decisions</th>
<th>Status</th>
</tr>
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<tbody>
<tr>
<td>Sept-2013</td>
<td><strong>Milestone:</strong></td>
<td>On track</td>
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<tr>
<td></td>
<td>- Test SiC modules to validate improvements in electrical and thermal performance.</td>
<td>- 50A/1200V SiC modules fabricated and tested;</td>
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<td></td>
<td>- Provide prototype modules for APEEM Projects.</td>
<td>- 100A modules are underway;</td>
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<tr>
<td></td>
<td></td>
<td>- 50A/1200V modules delivered</td>
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<tr>
<td>Sept-2013</td>
<td><strong>Go/No-Go decision:</strong></td>
<td>- On Track</td>
</tr>
<tr>
<td></td>
<td>- Determine if WBG modules can meet the targets on cost and reliability.</td>
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</table>
Approach/Strategy

- Replace Si devices with their SiC and GaN counterparts to promote their accelerated adoption in traction drive systems
- Develop innovative power module packaging to exploit the superior attributes of WBG power semiconductors
  - High power density
  - High frequency
  - High temperature
**Approach/Strategy**

**Packaging Performance Technical Parameters**

- **Criteria vs Technical Parameters**

\[
\frac{\$}{kW} \propto S_{Die\ Area} \cdot \left(1 - \eta\right) \cdot \frac{\theta_{ja,sp}}{(T_j - T_a)} \\
N_f = \alpha \cdot \left(\frac{1}{T_j - T_a}\right)^\beta \cdot \exp\left(\frac{E_a}{kT_m}\right) \\
\text{eff} = \eta \propto 1 - \left(\text{Pcon} + \text{Psw} + \text{Plp} + \text{Pr p}\right) / P
\]

**Packaging Electrical Parameters**

- **Packaging Thermal Parameters**

**Thermo-mechanical Parameters**

- Develop technical parameter basis and methodology to improve cost, power density, efficiency and reliability.
Approach/Strategy

- Prototype application specific modules to support system development efficiently
  - Designed power rating;
  - Unique architecture;
  - Optimal devices;
  - Functionality integration
  - Alternative form factor, etc.

Prototype Modules (75A/1200V Si) in Segmented Inverter (FY12, APE004)

Optimized layout modules (FY11, APE024)

SiC diode package (FY12, APE003)
Technical Accomplishments and Progress
Completed Module Packaging Design

- Completed Module Packaging Design
- Temperature distribution in an Integrated SiC power module
- Interconnection of power device dies in a 100A/1200V SiC power module
- Electric Schematics of a phase-leg module
- Power switch dies rated at 50A/1200V
- Interconnection of power device dies in a 50A/1200V SiC power module
- Interconnection of power device dies in a 100A/1200V SiC power module
- Temperature distribution in an Integrated SiC power module
Technical Accomplishments and Progress
Developed Packaging Process and Test Samples

- Developed Packaging Process and Test Samples
- EDS Analysis of Metallization

Co-package of Si-IGBT and SiC MOSFET
SiC MOSFET and Diode on Cold-Base Plate

Process Test_Bed
Technical Accomplishments and Progress
Performed Thermal Characterization

Schematics of thermal test setup

Thermal Resistance Comparison

Vf-T calibration curve of body diode in SiC MOSFET

Vf decay of body diode in SiC MOSFET during cooling down phase

$y = -2.45x + 900.25$
$R^2 = 0.9988$

Vf (mV)

Temperature (°C)

Time (µS)

Vf (V)

$R_{ja,sp}(cm^2°C/W)$

Conventional: 0.68
Integrated: 0.45
Technical Accomplishments and Progress

Performed Electrical Characterization

SiC module under electrical testing  SiC module Switching Waveforms  I-V characteristics

SiC module Turn-on Waveforms  SiC module Turn-off Waveforms  SiC module Switching Power Loss
Technical Accomplishments and Progress
Fabricated Module Prototypes

50A SiC Phase-leg/Conventional Cooling

50A SiC Phase-leg/Integrated Cooling

50A Si Phase-leg/Conventional Cooling

50A Si Phase-leg/Integrated Cooling
Technical Accomplishments and Progress
Validated Module Packaging Advancement

Comparison of SiC and Si Power Device

- SiC power device compared to Si one
  - 55% die size
  - 60% conduction power loss
  - 20% switching power loss

Comparison of new packaging (NP) to conventional (SOA) one

- New packaging compared to conventional (SOA)
  - 35% thermal resistance reduction
  - Decreased inductance by 50%
  - Decreased resistance by 30%
  - 30% overall volume and weight reduction
Technical Accomplishments and Progress
Evaluated Module Performance

Current density allowed for different power semiconductor and cooling combinations at $\Delta T_j=100^\circ$C for a typical operation ($D=0.5$, $f=5$kHz)

<table>
<thead>
<tr>
<th>Item</th>
<th>Si_Con. Cooling</th>
<th>SiC_Con. Cooling</th>
<th>Si_Integ. Cooling</th>
<th>SiC_Integ. Cooling</th>
</tr>
</thead>
<tbody>
<tr>
<td>Current Density $J_d$ ($A/cm^2$)</td>
<td>65.35</td>
<td>144.97</td>
<td>97.57</td>
<td>184.98</td>
</tr>
</tbody>
</table>
## Collaboration and Coordination

<table>
<thead>
<tr>
<th>Organization</th>
<th>Type of Collaboration/Coordination</th>
</tr>
</thead>
<tbody>
<tr>
<td>CREE</td>
<td>Source of SiC MOSFET and diode dies</td>
</tr>
<tr>
<td>Infineon</td>
<td>Source of Si semiconductor dies</td>
</tr>
<tr>
<td>International Rectifier</td>
<td>Source of Si semiconductor dies</td>
</tr>
<tr>
<td>Rogers/Curamik</td>
<td>Source of manufactured packaging component</td>
</tr>
<tr>
<td>University of Tennessee at Knoxville</td>
<td>Packaging component fabrication assistance</td>
</tr>
<tr>
<td>Virginia Tech University</td>
<td>Power electronics module packaging processes assistant</td>
</tr>
<tr>
<td>ORNL Materials Science and Technology Division/DOE VT Propulsion Materials Program</td>
<td>Packaging materials characterization</td>
</tr>
</tbody>
</table>
Proposed Future Work
Remainder of FY13

- Complete prototyping of all-SiC 100A/1200V power modules
  - Complete dual die paralleling study
  - Perform characterization of prototypes
  - Fabricate and deliver customer specific modules to APEEM team

- Develop high temperature packaging technology
  - Optimize high temperature die attach techniques
  - Develop high temperature multiple chips interconnection techniques
  - Conduct high temperature performance characterization of Si, SiC devices
  - Characterize high temperature packaging structures
Proposed Future Work
FY14 and Beyond

Complete packaging of high temperature WBG power modules
- Incorporate ORNL advanced bonding material/processing, encapsulate, thermal materials;
- Perform thermo-mechanical design and simulation of advanced module packages;
- Implement cost-effective materials and structures into WBG power modules;
- Conduct simulations and preliminary reliability tests of packages.

Complete packaging integration of intelligent WBG power modules
- Incorporate ORNL advanced high temperature gate drive circuitry
- Implement high temperature multi-chip module cooling technologies
- Optimize interconnection layout between control/drive and WBG power stage

Provide packaging support for other APEEM projects
- Deliver customer-specific prototypes to APEEM team for WBG power electronics systems development
Summary

• **Relevance:** Focused on achieving 40% cost reduction and 60% power density increase to facilitate DOE APEEM 2020 power electronics targets: $3.3/kW, 14.1kW/kg, 13.4kW/L.

• **Approach:** The approach being employed is to leap frog barriers of existing industrial baseline and bring innovative, systemic development to advance technologies.

• **Collaborations:** Latest industrial products and universities’ advanced research have been incorporated in the project. The achievements of this work are efficiently transferred to the industry through collaborations.

• **Technical Accomplishments:**

  Developed packaging technologies for advanced SiC automotive power modules, resulting in:

  - Compared power devices (SiC vs Si): 55% die size, 60% conduction power loss, 20% switching power loss
  - New packaging (relative to industrial SOA): 35% thermal resistance reduction, Decreased inductance by 50%, decreased resistance by 30%, reduced overall volume and weight by 30%
  - High temperature packaging techniques are undergoing fabricated application specific WBG modules:
    - All-SiC 50A/1200V phase-leg modules delivered for system evaluation
    - All-SiC 100A/1200V prototypes and customer specific modules are on track

• **Future Work:** Well planned, the components and materials have been prepared in advance. The more significant impacts can be achieved by following systemic research through prototypes delivery and transfer to industry.
Technical Back-Up Slides
Technical Accomplishments and Progress
Prepared Packaging Components

50A/1200V SiC MOSFET and SBD Diode Dies

50A/1200V Si IGBT and PiN Diode Dies

Cold_Base Plate

Conventional Base Plate

DBC Substrate
Technical Accomplishments and Progress
Performed System Evaluation

SiC Power Module Under Test at ORNL WBG Performance Evaluation Station

Temperature Dependence of I-V Curves of SiC MOSFET
Si Module Packaging Status and Trend

**Gen_I**
- Wire Bond
- Single Side Interfacial Cooling

**Inverter Assembly**

**Si Diode**
- Nissan LEAF®

**Si IGBT**

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**Gen_II**
- Planar Bond
- Integrated Cooling
- Reliability Enhancement

**Toyota Prius’10**

**Infineon HybridPack**

**Toyota LS600**

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**Gen_III**
- Dual Planar Bond
- Double Sided Cooling
- Integrated Double Sided Cooling

**Mitsubishi TPM**

**Semikron SKiN**

**Infineon .XT**

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**Hitachi DCPM**
SiC Module Packaging

- **CREE Phase-leg Module**
  - 1200V, 100A

- **Fuji 1200V/120A Phase-leg**

- **Powerex 100A/1200V/Phase leg**

- **Rohm 1200V/120A Phase-leg**

- **Infineon 1200V/30A JFET Phase-leg**

- **Mitsubishi Full SiC Module**
  - 1200V 800A 2in1

- **Mitsubishi Full SiC DIPPFC**
  - 600V/20Arms Interleave