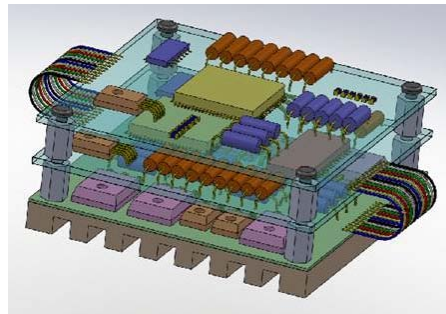
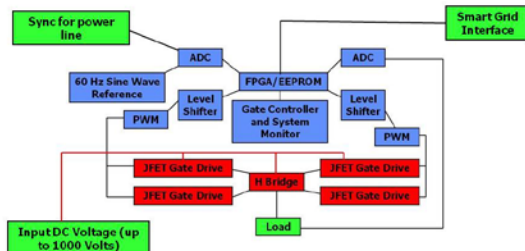


# Development of an Integrated Power Controller Based on HT SOI and SiC

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SAND 2010-7658C

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# Overview

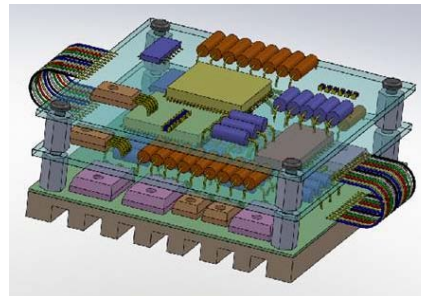
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- **Program Goals**
- **Accomplishments**
- **Design Details**
- **Test Results**
- **Conclusions**
- **Future work**

# Project Goals

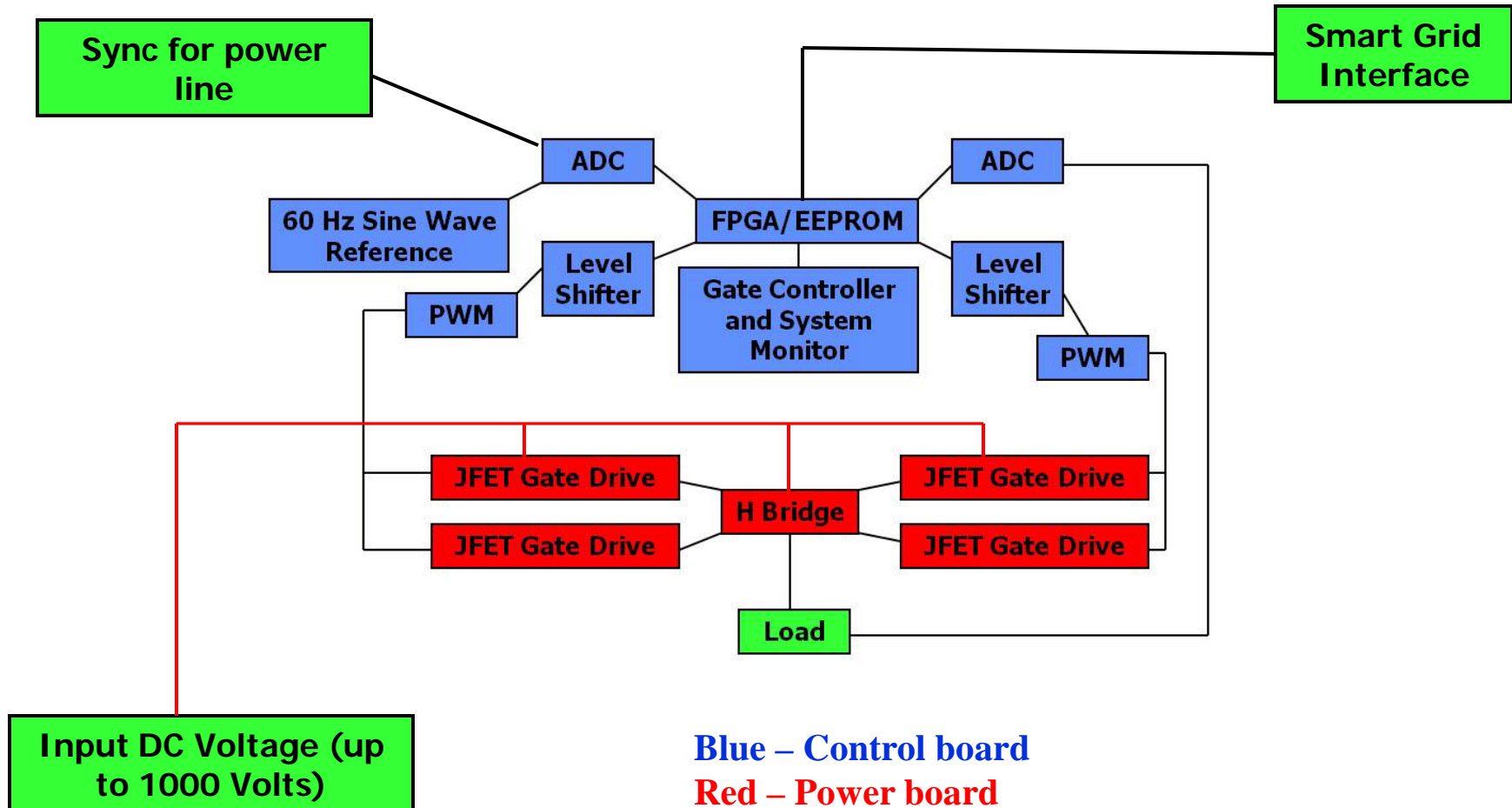
- **Design HT power controller that can be integrated into a single module**
  - **Benefits include:**
    - **Size reduction of power controllers**
      - Integration of the SOI based controller with (near) SiC power devices
    - **Ease thermal management requirements**
    - **Increase reliability**
      - Designed using HT components and elimination of board-level interconnects
    - **Increase efficiency**
      - Optimized to fully exploit the benefits of using SiC technology in power controllers
        - Can reduce energy losses by 3-4%
    - **High voltage capable designs**
- **Establish commercialization path to quicken the adaptation of energy-saving SiC technology**

HT - High Temperature  
SOI – Silicon-on-Insulator  
SiC – Silicon Carbide  
JFET – Junction Field-Effect Transistor  
PWM – Pulse Width Modulation  
MCM – MultiChip Module



Phase 3

# Block Diagram of the Power Controller

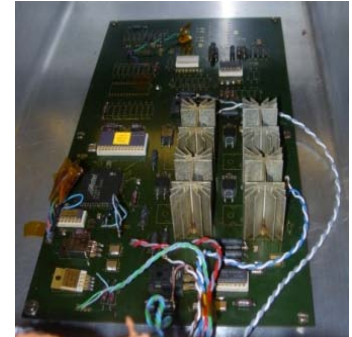


# Phase I Accomplishments

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Program Start Date FY09

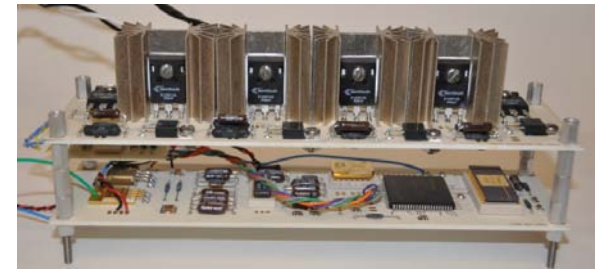
- **Successfully demonstrated a prototype microcontroller-based HT power controller at 240C**
  - Included basic safety functions to protect power devices
- **Demonstrated SOI gate drive for the JFET power devices**
- **Successfully tested SOI MESFET (Metal-Semiconductor-Field-Effect-Transistor) gate drive**



By combining SOI control and drive circuits with SiC, an intelligent system capable of operation up to 240°C (JFET junction temperature approaching 300°C) was successfully demonstrated

# Phase II and III Accomplishments

- **“Fine-Tune” prototype design**
  - **Designed, fabricated and tested a version 2 board with optimized system efficiency**
    - **Enhanced high side gate drive of the H bridge**
    - **Mitigated the current spikes**
    - **Minimized the switching “dead time”**
    - **Optimized the output filter**
    - **Improved microcontroller design**
      - **Better control of the power devices**
      - **Active feedback investigated; refinement required**
- **Started evaluation of APEI (Arkansas Power Electronics International) power module**
  - **Verified compatibility with Sandia’s controller**
  - **Performed 5 kW tests at APEI (room temperature)**
  - **Initiated oven tests with modules**
- **Contracted with Honeywell to program HT FPGA (Field Programmable Gate Array) with Sandia developed code – in progress**
- **Contracted with Life Bioscience to fabricate HT circuit board – in progress**



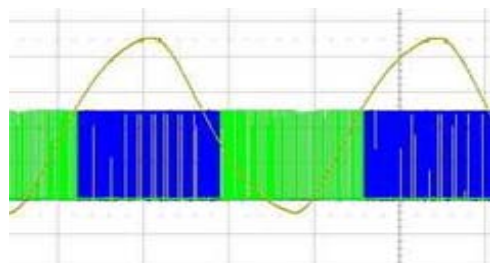
# Enhanced Performance - Improved Gate Drive

- **Enhanced switching methodology**

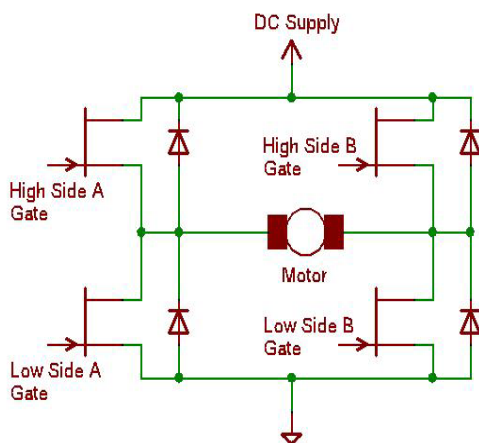
- **Three-level continuous PWM**

- **Voltage harmonics are both decreased in amplitude and increased in frequency**

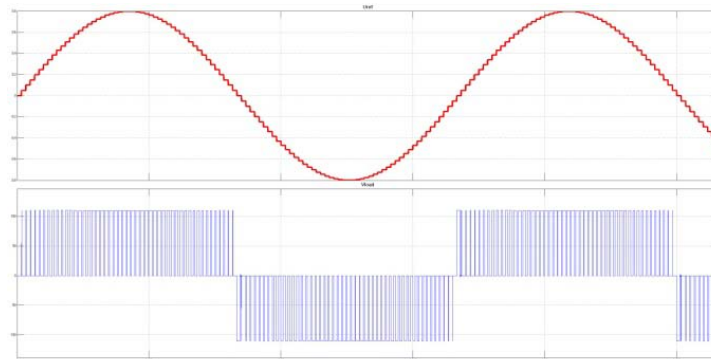
- **Reduced output filter size requirements (to achieve a given current THD)**
      - **Increased efficiency**



Prototype had PWM Gate Drive at Q1 and Q3; 60Hz at Q2 and Q4; Discontinuous PWM



Simulink Simulation



Enhanced circuit has PWM Gate Drive at Q1,Q2, Q3 and Q4; Three-level continuous PWM



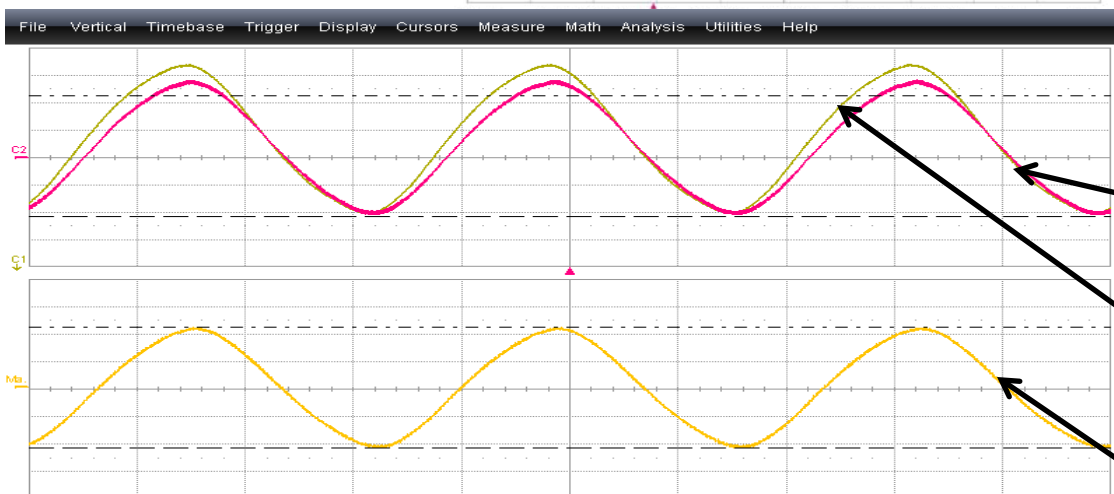
# Enhanced Performance - Improved Gate Drive

## Scope Image of PWM



Reference voltage (Red)

PWM (Yellow)



Output current (Red)

Reference voltage (Gold)

Output Voltage (Yellow)

<b>C1</b>	<b>FLT DC1M</b>	<b>C2</b>	<b>FLT DC</b>	<b>Math</b>	<b>(C4-C3)</b>	<b>Timebase</b>	<b>0.0 ms</b>	<b>Trigger</b>	<b>CS DC</b>
1.00 V/div	200 mA/div	5.00 V/div	5.00 ms/div			5.00 ms/div	Stop	18.0 V	
-4.3300 V	0.00 mA ofst	5.00 ms/div				500 kS	10 MS/s	Edge	Positive
6.57 V	448 mA	10.88 V							
2.17 V	-432 mA	-11.12 V							
Δy -4.40 V	Δy -880 mA	Δy -22.00 V							

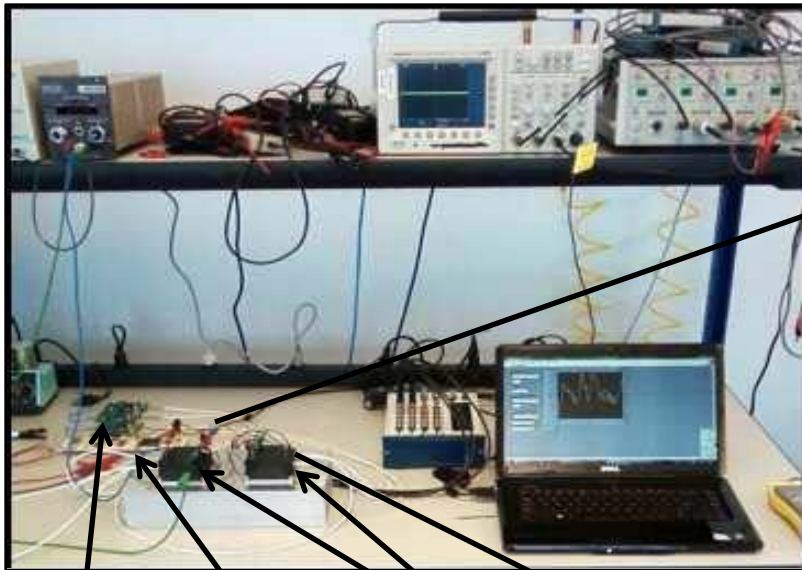
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## Scope Image of Output waveform



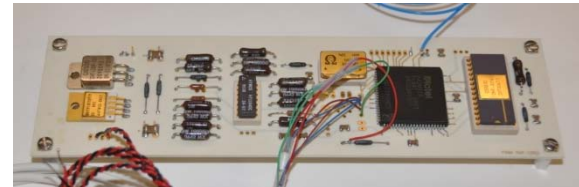
# Test Results – Initial Testing at APEI



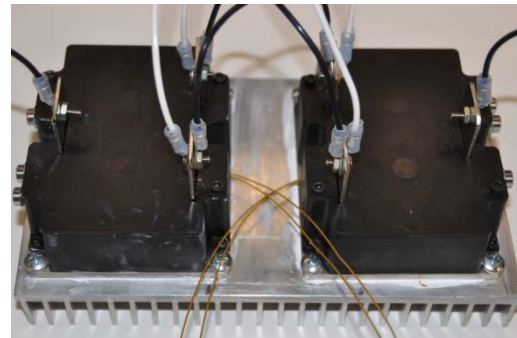
APEI  
Power  
Supplies

Sandia  
Controller

APEI  
Modules

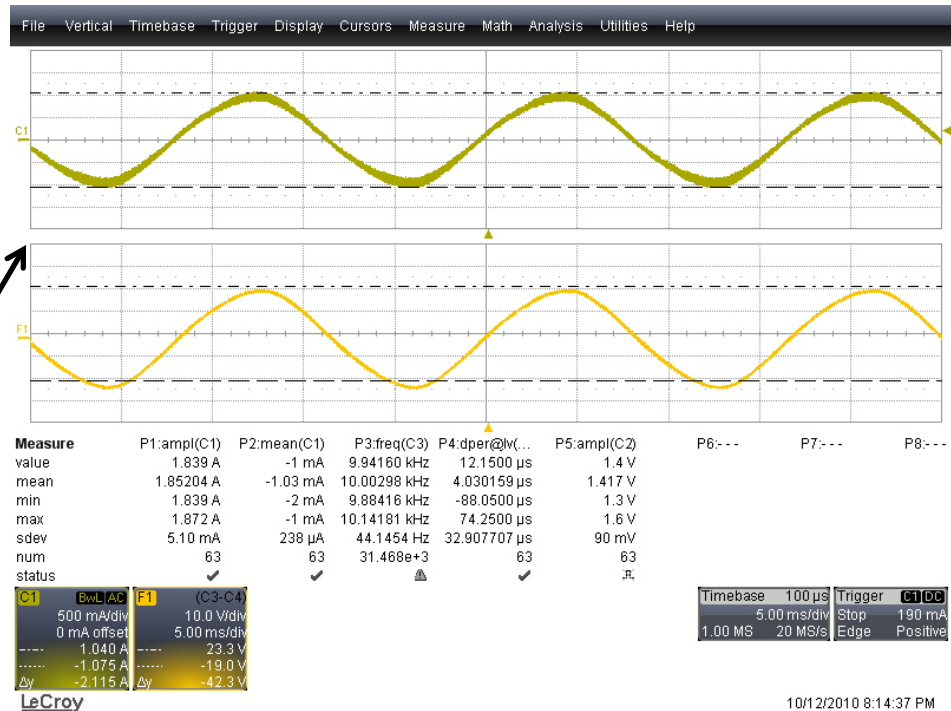
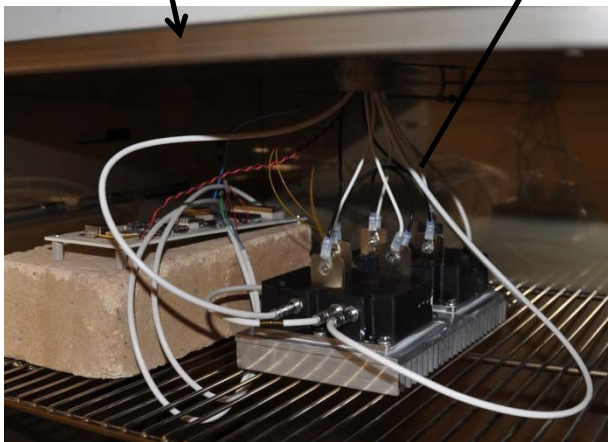
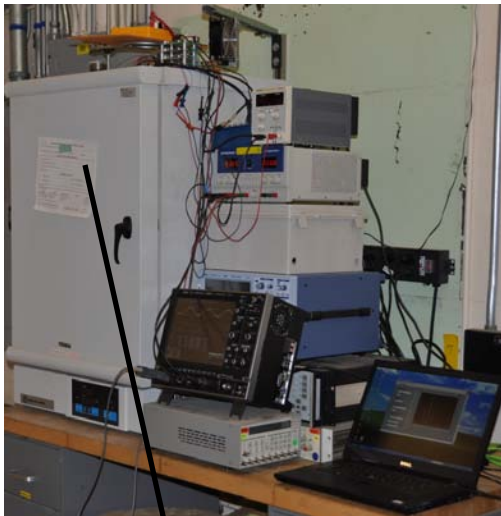


Sandia Controller



APEI Power  
module with  
integrated  
gate drive

# Initial Tests with APEI Power Module



Output Current

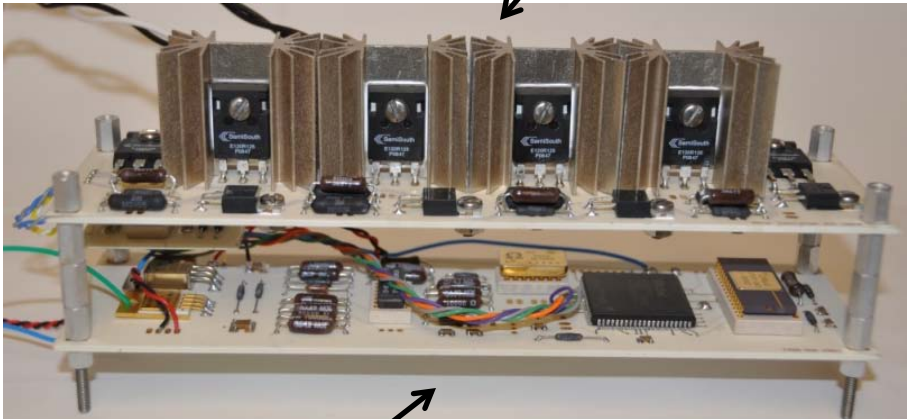
Output Voltage

Testing APEI modules with Sandia's controller at elevated temperatures

# Tests with JFET Power Board

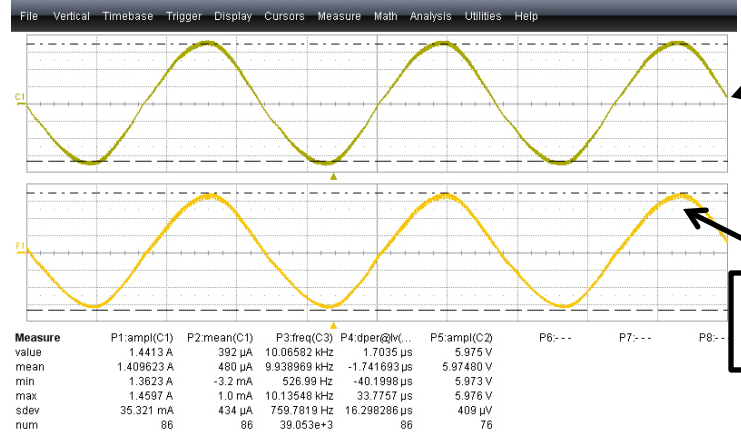


JFET Power Devices and Gate Drive



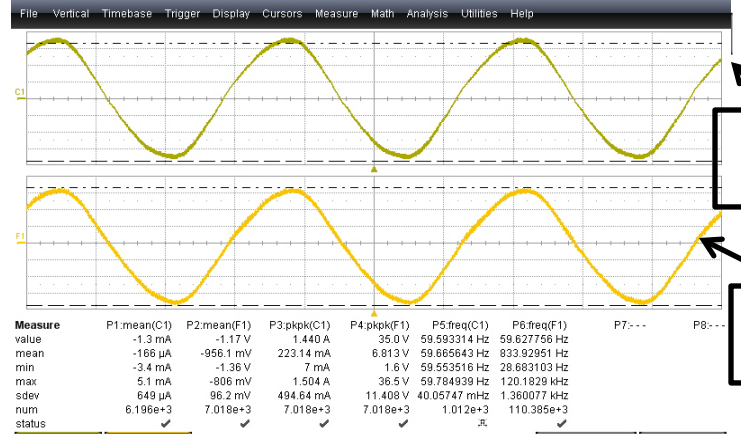
Controller

Resulting waveform at room temperature



Output Current

Output Voltage



Output Current

Output Voltage

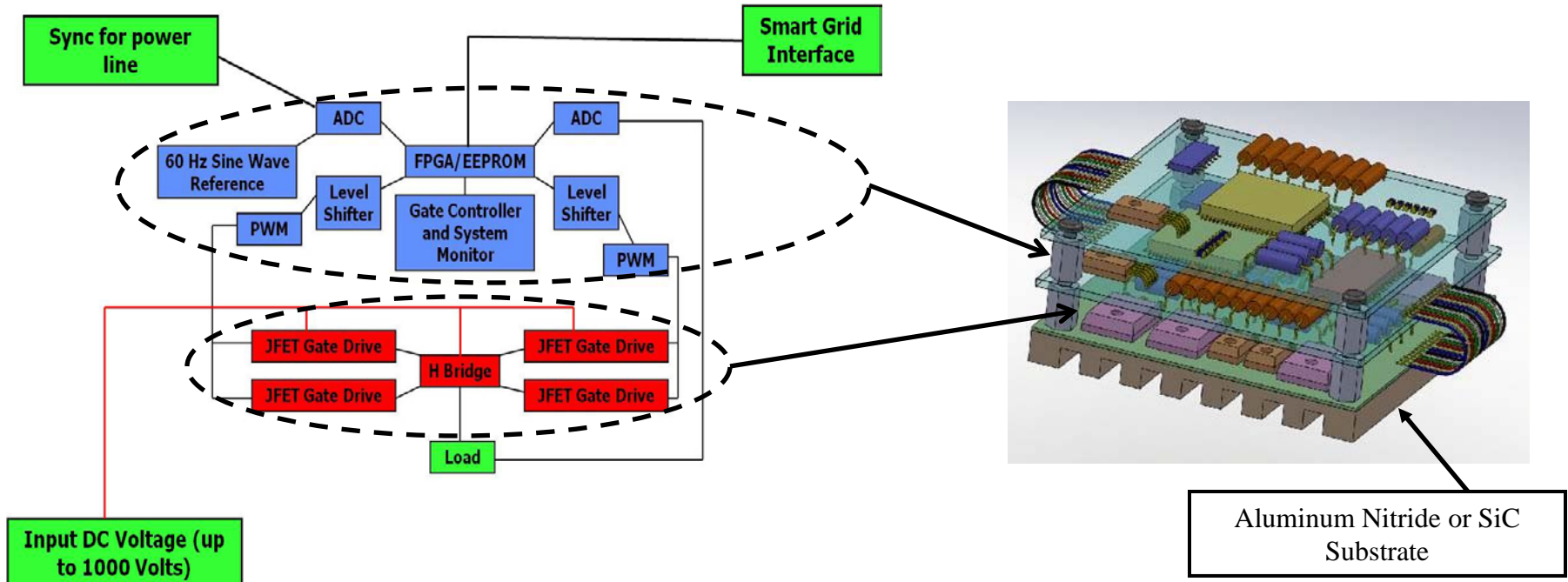
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 File Vertical Timebase Trigger Display Cursors Measure Math Analysis Utilities Help  
 Timebase 0.0ms Trigger 200  
 200 mA/div 5.00 V/div  
 0.00 mA/div 5.00 ms/div  
 500 ms 15.40 V  
 752 mA -18.80 V  
 -1.408 A -35.20 V

Resulting waveform at 200°C

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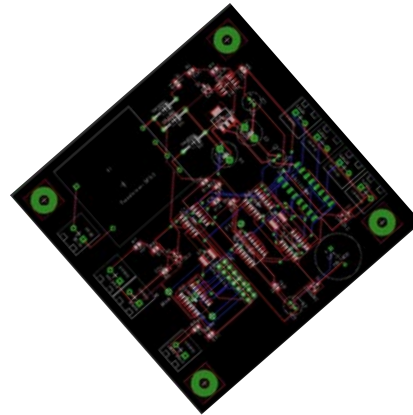
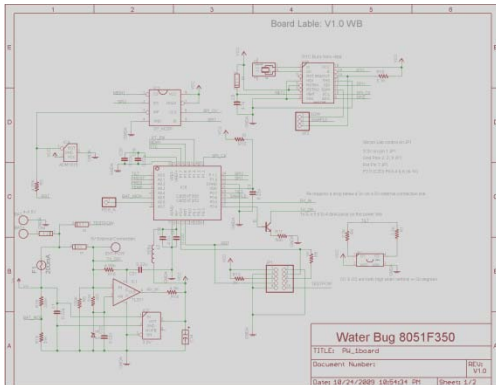


# Single Module Solution



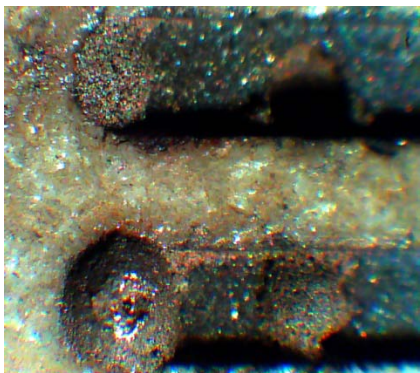
Investigating potentially utilizing same substrate for power devices and MultiChip Modules (MCM)

# New Extreme HT-HV Circuit Boards

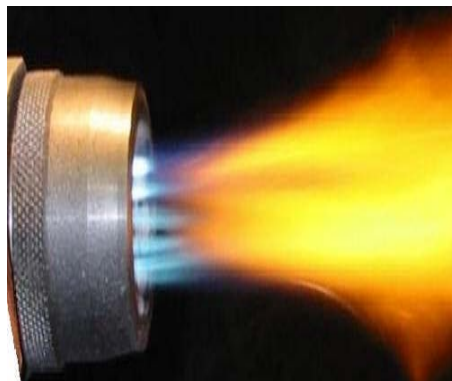


- % start
- G90,G71,G54
- M5, M6
- G92 0.001,0.200,-0.200
- G1 0.001,0.570,-0.200
- G1 0.456,0.200,-0.200
- G1 0.456,0.234,-0.200

Standard Schematic → Optical Image → **NEW** Convert Image to CNC G-Codes



**New** HT Lead Free Solder



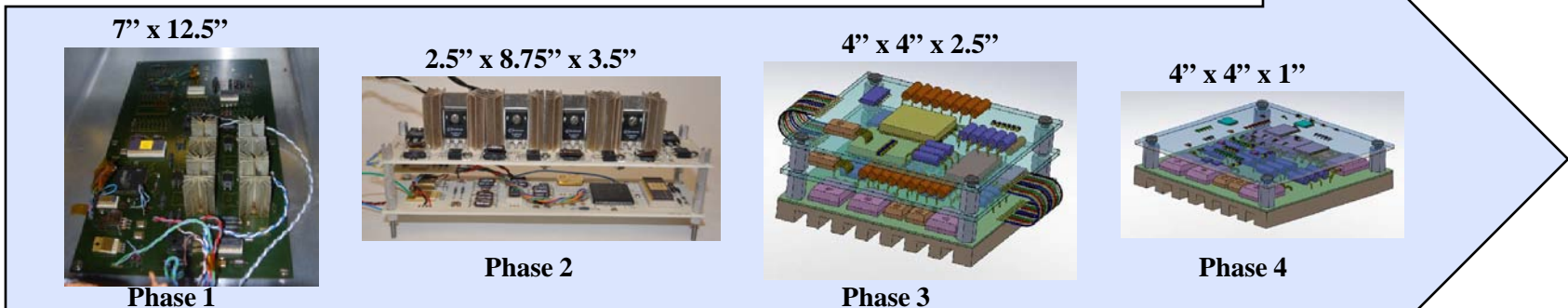
**New** Metalize Circuit Traces



**New** Fab SiC Circuit Board

# Conclusion

- Lab tested an enhanced controller board and a power board consisting of JFET power devices with gate drive
- Completed initial testing at APEI using APEI's power modules, LT gate drive power supply and Sandia's controller; 5kW tests
- Completed initial testing at Sandia at elevated temperatures
- In progress: conversion of Sandia code into a HT FPGA (Honeywell)
- In progress: fabrication of HT circuit board





## Future Plans

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- **Evaluate APEIs HT gate drive power supplies**
- **Investigate utilizing APEI's JFET power module with HT gate drive power supply and steps required to integrate into single module**
- **Refine feedback control**
- **Complete the design for MCM controller**
- **Evaluate Honeywell HT SOI FPGA**
- **Evaluate HT circuit board**
- **Demonstrate “next step” in single module solution (Sandia or APEI power boards)**





# Collaborative Effort with Academia and Industry

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- **DOE Funded**

- **Participants include:**

- **Sandia (Lead)**
    - **Arizona State University (Circuit simulation, fabrication of test circuits using HT) MESFET – JFET gate drive) - Phase I**
    - **University of Maryland – HT lead attach**
    - **PermaWorks (Inverter design simulation and fabrication of HV supply) – Phase I**
    - **APEI (Power modules, HT power supplies, thermal analysis) – Phase II, III**
    - **Life BioScience (HT circuit boards) – Phase II, III**

- **COTS suppliers**

- **Honeywell SSEC**
    - **Cissoid**
    - **SemiSouth**

The authors would like to thank DOE Energy Program and Imre Gyuk for financial support of this research.