Final Report

Project Title:	Vapor Transport Deposition for Thin Film III-V Photovoltaics
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Executive Summary:

Silicon, the dominant photovoltaic (PV) technology, is reaching its fundamental performance limits as a single absorber/junction technology. Higher efficiency devices are needed to reduce cost further because the balance of systems account for about two-thirds of the overall cost of the solar electricity. III-V semiconductors such as GaAs are used to make the highest-efficiency photovoltaic devices, but the costs of manufacture are much too high for non-concentrated terrestrial applications. The cost of III-V's is driven by two factors: (1) metal-organic chemical vapor deposition (MOCVD), the dominant growth technology, employs expensive, toxic and pyrophoric gas-phase precursors, and (2) the growth substrates conventionally required for high-performance devices are monocrystalline III-V wafers.

The primary goal of this project was to show that close-spaced vapor transport (CSVT), using water vapor as a transport agent, is a scalable deposition technology for growing low-cost epitaxial III-V photovoltaic devices. The secondary goal was to integrate those devices on Si substrates for high-efficiency tandem applications using interface nanopatterning to address the lattice mismatch. In the first task, we developed a CSVT process that used only safe solid-source powder precursors to grow epitaxial GaAs with controlled *n* and *p* doping and mobilities/lifetimes similar to that obtainable via MOCVD. Using photoelectrochemical characterization, we showed that the best material had near unity internal quantum efficiency for carrier collection and minority carrier diffusions lengths in of ~ 8 μm, suitable for PV devices with >25% efficiency. In the second task we developed the first *pn* junction photovoltaics using CSVT and showed unpassivated structures with open circuit photovoltages > 915 mV and internal quantum efficiencies >0.9. We also characterized morphological and electrical defects and identified routes to reduce those defects. In task three we grew epitaxial ternary $GaAs_xP_{1-x}$ and $In_{0.5}Ga_{0.5}P$ alloys, with composition set by the ratio of GaAs/GaP or InP/GaP mixed as the source powder. $GaAs_{0.3}P_{0.7}$ has the appropriate bandgap to serve as a top cell on Si and $In_{0.5}Ga_{0.5}P$ is near the composition used as a surface passivation layer on GaAs *pn* junction photovoltaics. In the final task we demonstrated III-V selective area epitaxy using CSVT as a first step toward the growth of III-V micro- or nanostructures for an integrated tandem solar cell on Si. We also found that direct epitaxial growth on Si appears to be impossible in the current H_2O-CSVT reactor design, likely due to the formation of SiO_x.

This work sets the stage for targeted development of an improved CSVT process and for the scale up of the proof-of-concept work from a research to manufacturing-relevant platform. Replacing H_2O as a transport agent with HCl would provide the ability to deposit directly on Si by avoiding oxide formation and to allow for the deposition of Al-containing alloys that would otherwise oxidize. Improved engineering design and implementation of an in-line multi-station CSVT would allow for direct deposition of device structures in a single system.

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Background

The use of III-V materials for solar energy conversion is compelling. High coefficients of light absorption along with tunable bandgaps and lattice constants have resulted in record conversion efficiencies for both one-sun and concentrator photovoltaic (PV) applications. GaAs, for example, has been used to manufacture single-junction PVs with world-record efficiencies of 28.8% at one sun.[1] However, the cost of III-V solar cells has prevented them from entering the marketplace except in specialized applications such as use in space and in concentrators with sun trackers.

Currently, Si cells dominate the market. As PV manufacturing costs have plummeted, technologies to increase efficiency have become critical. With module costs below \$150 m^{-2}, total installed system costs are more-impacted by efficiency increases than by foreseeable reductions in areal cost. Si cell efficiencies are nearing theoretical limits and Si PV modules are unlikely to reach the 25-30% efficiency range.[2]

Tandems on Si have long been an obvious route to high-efficiency devices, but progress has been slow as there is a lack of PV-quality semiconductors with a band gap of 1.7-1.8 eV needed for a current-matched top cell on Si. For example, the efficiency of CIGS-based chalcopyrite semiconductors is poor when the band gap is increased due to native defects.[3] The II-VIs have been explored, but larger-gap materials such as $CdSe_xTe_{1-x}$ have not yet provided efficient cells, even in MBE-grown epilayers.[4] Recent work on lead-halide perovskites is promising, but their stability to moisture and temperature is limited and efficiencies for compositions with suitable band gaps are low.[5] III-Vs, particularly $GaAs_{1-x}P_x$ and $In_{1-x}Ga_xP$, are able to provide high-efficiency, stable, appropriate band-gap materials to serve as a top cell on Si.[8] However, costs for III-Vs must be dramatically reduced to enable them to serve energy market demands.

III-V PV costs are controlled by two factors: semiconductor growth and the substrate. The dominant growth technologies, MBE and MOCVD, are much too expensive (as described in the background section below). Single crystal substrates are also prohibitively expensive, impeding the expansion of III-V solar technologies. New deposition methods must also look forward, toward compatibility with inexpensive substrate technologies, like Si.

Here, we describe a very different approach to III-V deposition based on close-space vapor transport (CSVT). The approach uses only safe, solid-source precursors and is capable of depositing at high rates (>1 μm/min) with precursor utilization efficiency near 100%. We also describe *pn* solar cell devices fabricated by CSVT, the deposition and properties of ternary III-V's by CSVT, and efforts to deposit directly on Si using a patterned interface.

Prior to the detailed discussion of CSVT deposition, we first briefly examine current commercialized technologies for III-V growth as well as related lower-cost technologies that are currently in the research stage to provide context for the CSVT technology developed here.

Commercial Technologies for III-V deposition

a) MBE and MOCVD

Epitaxial growth of III-V materials is currently dominated by two techniques: molecular beam epitaxy (MBE) and metal-organic chemical vapor deposition (MOCVD).

Neither of these techniques is well-suited to large-scale production, though the technology is very mature and very high quality films can be grown with precise control of doping and composition. MOCVD costs are high due to the expense and low utilization (~30%) of precursors, modest growth rates (< ~100 nm min^{-1}), equipment complexity, and safety infrastructure needed to handle toxic, pyrophoric gases.[6] MBE costs are high due to slow growth rates and limitations of scalability.

It is very unlikely that costs using such technology can be lowered to be competitive for terrestrial non-concentrated applications (i.e. ~\$0.5/W_p or ~\$100/m^2, W_p is a peak watt). In fact, a recent study by NREL indicates that both radically new deposition and substrate technologies will be needed to lower costs sufficiently to reach the targets of ~\$0.5/W_p that will make the technology competitive with fossil-fuel derived electricity.[7] Recent advances in MBE/MOCVD growth on Si substrates, for example through the use of graded buffer strain release layers, may be leveraged through similar device designs in a CSVT-based approach.[8]

b) Liquid Phase Epitaxy

Liquid phase epitaxy (LPE) is an older commercialized technology for III-V growth. It relies on controlled crystal growth from supersaturated molten metal solutions under near equilibrium conditions. It is still used for the growth of light-emitting diodes.[9] Homo- and heterojunction junctions and devices are possible, but have historically been difficult to control.[10] More research in high-volume, low cost LPE approaches would be needed to understand viability for solar photovoltaics.

Alternative growth techniques for scalability and cost reduction

a) Hydride vapor phase epitaxy (HVPE)

HVPE is commonly used for the growth of GaN films but has historically not been favored for production of III-V-based photovoltaics. Recently, the National Renewable Energy Laboratory (NREL) has revived the development of the technique. The HVPE reactor at NREL is comprised of a custom fused quartz chamber through which H_2 is flowed as a carrier gas. As with MOCVD, the source of arsenic for HVPE is AsH_3, though the overpressure required is reportedly lower. The group III precursors are introduced as pure metals in a heated boat upstream of the deposition zone, and are transported using HCl gas. Typically, source temperatures are ~700 °C. High growth rates above >1 μm have been achieved with no large degradation in crystal quality. Doping is accomplished with metal-organic compounds introduced in the gas phase.

In contrast to MOCVD, compositional grading in HVPE is achieved by varying the amount of transport agent added to the metal source streams. Binary and ternary compounds containing In and P have also been reported, suggesting that it could be applied to tandem or multijunction PV structures in a similar fashion as MOCVD. Deposition of Al-containing compounds has traditionally been a challenge due to the high reactivity of the chlorides with the fused silica reactor walls as well as its affinity for oxygen,[11] though there is no fundamental reason why deposition of Al-containing compounds cannot be accomplished.

HVPE advantages relative to MOCVD include the possibility for faster growth (similar to CSVT, discussed here), and the use of a less-expensive metallic Ga precursor. The material quality (e.g. mobility as a function of carrier concentration)

reported are similar to MOCVD and to what we have shown below with CSVT. Significant device development has been accomplished to date for HVPE; $In_{1-x}Ga_xP$ passivated GaAs homojunction devices with efficiencies near 16% have been reported.[12]

HVPE also has its challenges. It uses toxic arsine/phospine as the group V precursor and requires engineered gas flow for uniform precursor delivery.[13] HVPE is thus likely to require similar equipment expense as MOCVD and have similar limitations in precursor-utilization to probably near ~30%. In order to fabricate abrupt junctions, multiple in-line growth chambers have been used to avoid temperature transients.[13]

b) Thin-film vapor-liquid-solid (TF-VLS) growth

TF-VLS growth is a technique developed recently for growing films on non-epitaxial substrates.[14] Heterojunction devices fabricated by the Javey group at University of California Berkeley using *p*-InP absorbers have reached efficiencies of 12%. In this technique, indium metal is first deposited onto Mo foil or sputtered Mo on SiO_2/Si, then capped by SiO_x and exposed to a PH_3:H_2 flux at 750 °C and 100 Torr which initiates a dendritic growth mechanism under the capping layer. After the initial dendrites coalesce, grain sizes in the final films can be in excess of 100 μm. Devices are fabricated by depositing a window of *n*-TiO_2 and a transparent conductive oxide contact layer.

Though indium is expensive, it could be electrochemically deposited in a high-throughput process with near-unity utilization, and only a thin film is required. However, there are no reports of other III-V compounds deposited by TF-VLS, and no simple approach for fabricating tandem or multijunction devices. The best V_{oc} reported for InP solar cells under one-sun equivalent illumination is 692 mV, implying a voltage deficit of ~650 mV relative to the band gap. Further development may allow TF-VLS to compete in efficiency with other more-established technologies, such as CdTe or CIGS, but as a polycrystalline approach using metal foil substrates it is unlikely to compete in efficiency with single-crystalline III-V technology.

Review of CSVT

CSVT was invented by Nicholl in 1963[15] as a variant of the vapor transport methods which use low-cost solid precursors. The innovation of placing the substrate in close proximity to the source provides increased growth rates and improves precursor and transport-agent utilization. Nicholl reported the growth of GaAs, Ge, and GaP.[16] This work was followed over the next fifteen years with demonstrations of epitaxy of InP,[17] GaAsP,[18] and ZnSe,[19] as well as further characterization of GaAs, GaP,[20] and Ge.[21] Often the transport agent for CSVT was H_2O, which reacts with the Group III element to form a volatile oxide and liberates a volatile dimer or tetramer of the Group V element, eliminating the need for pyrophoric metal-organic and toxic hydride species. Other transport agents included HCl and I_2.[22] In all cases, the reaction is expected to be fully reversible and thus materials utilization should approach 100% with the appropriate reactor geometry.[15]

The applicability of these films for semiconductor devices was not thoroughly investigated, and few reports of materials electronic properties from this period exist. For GaAs, carrier concentration and majority carrier mobility were measured, but the properties essential to PV were not characterized. In 1967, the first CSVT devices, including Schottky junction solar cells, were fabricated from polycrystalline GaAs films on metal foil substrates.[23] Homojunction devices were attempted but had negligible photovoltaic response and no electrical properties were reported for those devices.

CSVT continued to be explored for single-crystal semiconductor growth through the 1990s. Models of CSVT growth of GaAs were published in the 80s,[24] including one proposed by Côté and Dodelet in which the equilibrium concentrations of As_4, As_2, and Ga_2O entirely determine the growth rate.[25] Studies performed in the late 80s and early 90s using deep level transient spectroscopy (DLTS) of Schottky diodes on *n*-type GaAs films found that the well-known GaAs "EL2" defect level arising from As antisite complexes is present in CSVT material at low concentrations which vary with growth temperature[26–28] and rate.[29] This is consistent with growth rate being limited by Ga_2O diffusion, leading to As-rich films as in the model of Côté and Dodelet. Other studies used secondary ion mass spectrometry (SIMS) to correlate photoluminescence (PL) peaks with elemental impurities.[30,31] In the late 90s into the 2000s, there was an increased interest in CSVT for GaAs PVs. This included some reports of GaAs grown *via* selective area epitaxy (SAE) on Si using H_2O as a transport agent, but as described below we were unable to reproduce this work.[32]

The history of CSVT has demonstrated that the technique has limitations due to its use of solid sources – such as its applicability to complex, low-dimensional structures – but it is well-suited to the simpler structures needed for PV. Doped CSVT-grown films had been demonstrated. Many studies found Si to be a dominant shallow donor,[25,31,33] in contrast to our own work in which Si has never been detected (using SIMS) in the bulk of CSVT films. We view the latter result as more reliable given the low volatility of Si and its oxides. This also provides a simpler explanation for low carrier concentrations in films grown from Si-doped sources as observed in the literature.[33] Transport efficiencies of other dopants (e.g., Zn, Te, Ge) were also established.

Although doping had been demonstrated in CSVT, the use of low-cost powder sources to control it was limited. The literature also lacked quantification of the minority carrier properties which are essential for solar cell device applications, and there was little information on the electrical and crystalline quality of the films grown *via* CSVT. Most importantly, homojunction solar cell devices fabricated using CSVT had not been demonstrated.

Prior reports of CSVT $GaAs_{1-x}P_x$ growth generally explored the composition and growth rate of the material but did not provide electronic characterization.[18,34] The only report of electronic characteristics from this early work is of p^+-$GaAs_{0.8}P_{0.2}$ with a low majority carrier mobility.[35] The crystalline quality of these materials was not characterized, and the relationship between source and film [P] (from mechanically ground GaAs/GaP mixtures,[18,35] or melt-grown $GaAs_{1-x}P_x$)[18] was not established.

Only a few reports of SAE exist in the CSVT literature; these utilize large-scale patterns (35 × 35 μm) for GaAs-on-Si heteroepitaxy.[32,36] However, these reports utilize H_2O as a transport agent, and our experience shows that the Si surface irreversibly oxidizes before epitaxial growth can occur. Micro- or nanoscale selective-area

homoepitaxy has not been demonstrated using CSVT. Patterned growth at this smaller scale is important both to enable III-V on Si heteroepitaxy in the future, using a halide transport agent (which would leave the Si surface unoxidized), and as a route to exploring CSVT growth dynamics.

Summary of Statement of Project Objectives, Milestones, and Go/No-Go points

Budget Period 1 (18 months)

Task 1. Deposit high-quality *p* and *n*-type GaAs by vapor transport on epi-GaAs

ST-1.1: Deposition of p-type films and improved n-type films

> **Milestone: Deposit CSVT GaAs with *p*-type doping controllable from 10^{17} cm^{-3} to 10^{19} cm^{-3} via Zn incorporation into source**

We demonstrated that *n*- and *p*-type doping can be achieved by addition of metallic dopants to mechanically-ground GaAs. Powder containing controlled amounts Te, Ge, or Zn were pressed into pellets and used as source material in the CSVT reactor. Results of the Zn doping study were published.[37]

ST-1.2: Photoelectrochemical characterization of single film to determine diffusion lengths and photovoltages and growth optimization

Current-voltage characteristics, dopant densities, and internal quantum efficiency were measured using ferrocene/ferrocenium non-aqueous electrochemistry; dopant densities and mobilities were also routinely measured using Hall effect. Characterization of *n*-type films was published[37] and showed electrical quality on par with MOCVD-grown films.

ST-1.3 Defect and electrical characterization

> **Milestone: Demonstration of L_d >2 μm from CSVT GaAs film via growth parameter optimization**

Moderately-doped (~10^{17} cm^{-3}) *p*-type films were found to exceed 5 μm electron diffusion lengths without additional growth optimization, with the primary challenge being a reduction in the unintentional background impurity incorporation. Sulfur from the graphite heaters was found to be the most common unintentional *n*-type dopant, limiting the minimum achievable carrier concentration to ~5 × 10^{16} cm^{-3}.

Task 2. Fabricate, test, and optimize epitaxial pn junction devices

ST-2.1: Device simulations of pn GaAs using 1D device physics simulators PC1D and/or AMPS with measured materials and junction parameters

Preliminary device simulations using measured L_D suggest that CSVT devices based on existing materials can exceed 25% efficiency. Measured quantum efficiency curves were generally consistent with PEC spectral response measurements as well as simulated curves. This allowed us to tune the emitter thickness for improved current collection.

ST-2.2: Fabrication of CSVT GaAs n^+p and p^+n solar cell devices via the sequential deposition of material

We chose to focus on fabrication of n^+p devices due to the lower transport efficiency of Zn and the higher diffusion length for minority electrons. Initial devices used ~5×10^{17} cm^{-3} Zn wafers as the absorber so that emitter growth parameters could be optimized prior to attempting the more time-intensive sequential deposition.

ST-2.3: Characterize PV performance and dopant profiles to incorporate into computer simulations and to improve performance

> **Milestone and Go/No-Go: Demonstrate GaAs solid-state PV with internal quantum efficiency > 0.95 and V_{oc} > 0.95 V**

Prior to the go/no-go decision, we were able to demonstrate *the first complete GaAs pn junction devices with CSVT absorber and emitter films*. By etching the emitter to ideal thickness we measured an IQE > 90%. The best V_{oc} > 900 mV was achieved by a device with a wafer absorber and without surface passivation. Following the go/no-go decision, CSVT absorber devices have surpassed those with wafer absorbers with record V_{oc} > 915 mV.

<u>Budget Period 2 (18 months)</u>

Task 3: Develop transport conditions for $GaAs_{1-x}P_x$ deposition and optimize properties

ST-3.1: Grow $GaAs_{1-x}P_x$ with x from 0.2 to 0.8 on GaAs and determine the dependence of x on source composition and transport conditions

Using mixed GaAs/GaP powder sources, we grew $GaAs_{1-x}P_x$ films with 0.25 < x < 0.65 and ~90% [P] of the source. Film [P] showed no dependence on temperature and all films were epitaxial and aligned to the GaAs (100) substrates.

ST-3.2: $GaAs_{1-x}P_x$ characterization using photoelectrochemistry and PL/Hall measurements to determine suitability as an absorber and/or thin top window layer for GaAs cell.

> **Milestone (Task 3): $GaAs_{1-x}P_x$ (0.2 < x < 0.8) deposited by CSVT on GaAs wafers with doping concentrations of 10^{17}- 10^{18} cm^{-3} with PEC response, lifetime and mobility characterized.**

Following the methods from ST-1.2, non-aqueous photoelectrochemical measurements and Hall effect were used to assess electronic quality of $GaAs_{1-x}P_x$. The desired N_D was reached and this work was published.[38] Although diffusion lengths for direct E_g compositions of $GaAs_{1-x}P_x$ were between 100 and 200 nm were below the threshold for integration into a device (due to misfit dislocations), we measured best short-circuit photocurrent of 6.7 mA cm^{-2} and open-circuit photovoltage of 0.915 V for *n*-$GaAs_{0.7}P_{0.3}$ with $N_D = 2 \times 10^{17}$ cm^{-3}.

Task 4: Nanopatterning to enable deposition of high-performance III-Vs on Si

The planned approach to this task was to deposit GaAs on Si substrates *via* selective-area epitaxy. Although there are reports of CSVT GaAs-on-Si heteroepitaxy,[36] we were only able to obtain polycrystalline nucleation, likely a result of the H_2O ambient driving oxidation of the Si surface. We therefore explored several alternative approaches described below.

ST-4.1: Demonstrate selective growth of GaAs on patterned Si wafers.

GaAs-on-GaAs selective area growth was optimized for (111)B and (100) GaAs surfaces and reproducible 1 cm^2 areas of high quality microstructures were fabricated. Selective area heteroepitaxy was also probed with the growth of $GaAs_{0.7}P_{0.3}$ on patterned GaAs. Patterned virtual Ge substrates were successfully used as an interlayer in the deposition of GaAs on Si.

ST-4.2: Characterize patterned GaAs on Si using PEC contacts, TEM, PL, and x-ray diffraction. Correlate defect density with photovoltage and quantum efficiency for carrier collection, and use information to improve materials properties.

> **Milestone: Demonstrate internal quantum efficiency for GaAs on Si > 0.95 in PEC cells and photovoltages similar to planar controls > 800 mV.**

Characterization of GaAs-on-GaAs microstructures is nearing completion. These *n*-type materials show good photovoltages and high photocurrents. Work on GaAs-on-Ge microstructures is ongoing.

ST-4.3: Fabricate pn junction PVs from nanopatterned GaAs on Si by sequential VT deposition of base, emitter and window layer.

Due to the limitations of H_2O-CSVT for growth on Si, we have not begun direct work on this task. We propose that the best strategy for growth on Si using CSVT is to replace the H_2O transport agent with a halide; the development of such a system is currently under way. We will leverage the knowledge gained from our current work on this task in addition to a new growth reactor in order to achieve this goal.

Final Deliverables

Final Deliverable 1: Solid-state *pn* junction GaAs solar cell on patterned SiO_2/Si wafers with internal quantum efficiency > 0.95 and V_{OC} > 0.9.
This deliverable was not completed due to the inherent problems with growing on Si substrates using a H_2O-mediated transport method. We believe that a chloride-CSVT system will enable us to overcome this barrier in future work.

Final Deliverable 2: Photoelectrochemical semiconductor solar absorber testing facilities and standard protocols available to all users of the Molecular Foundry.
These facilities and protocols are now well-established and available to users at the Molecular Foundry.

Project Results and Discussion

As outlined in the statement of project objectives summary above, the project consists of four main tasks, which aim to (1) grow single-layer homoepitaxial thin films with controlled *p* and *n* doping and excellent materials quality, (2) combine *p* and *n*-type films to make prototype *pn* junction test devices and demonstrate performance metrics comparable to established growth technologies, (3) use mixed powdered sources to grow ternary $GaAs_{1-x}P_x$ with control over the bandgap, (4) demonstrate CSVT is compatibility with interface nanopatterning strategies for strain-relief on lattice mismatched Si substrates. We chose these ambitious tasks because they all contribute directly to the vision for a low-cost top cell, integrated with a Si bottom cell, capable of achieving at least 30% efficiency under one sun illumination.

We first constructed a simple CSVT reactor, illustrated in Figure 1. The reactor is similar in design to those described in the literature,[22,25,39,40] using H_2 as a carrier gas and H_2O as the transport agent needed to volatilize group III elements. The transport reaction is primarily determined by the equilibria

$$\mathbf{2GaAs(s) + H_2O(g) \rightleftharpoons Ga_2O(g) + As_2(g) + H_2(g)}$$

$$\mathbf{2GaAs(s) + H_2O(g) \rightleftharpoons Ga_2O(g) + \tfrac{1}{2}\, As_4(g) + H_2(g)}$$

A temperature gradient of 10 to 50 °C drives the diffusive transport of gas-phase species towards the cooler single-crystal GaAs substrate, where supersaturation causes the growth of an epitaxial film. Because there is no flow, the transport agent is not consumed and no flow engineering is needed, in contrast to that needed for MOCVD or HVPE technologies. The use of solid sources puts the CSVT process in a similar potential cost category as sputter or vapor transport, as used for CdTe deposition.[41]

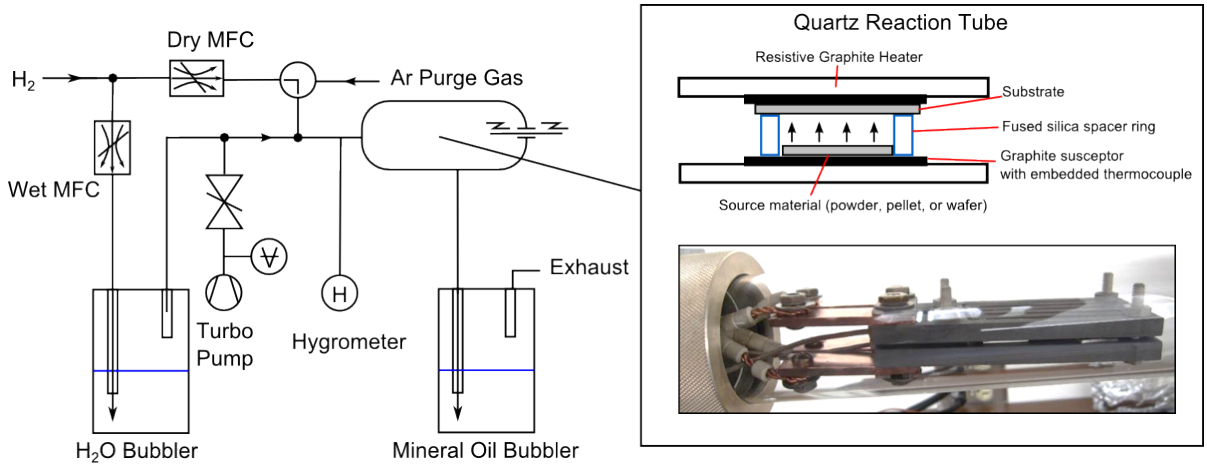

Figure 1: Schematic diagram of the custom CSVT reactor and reaction zone. Hydrogen gas containing water vapor reacts with GaAs to create volatile species in-situ. A temperature gradient between the

source and substrate drives the mass transport of these species and causes GaAs to redeposit on the cooler substrate. Temperature is monitored throughout the reaction by thermocouples (TC).

Task 1: Deposit high-quality *p* and *n*-type GaAs by vapor transport on epi-GaAs

Doping and film characterization (Subtask 1.1)

In choosing dopants, either the elemental form or the predominant oxide species must be volatile within the range of source temperatures used for growth. Additionally, it is desirable for the dopants to diffuse slowly such that abrupt dopant profiles can be achieved. For *n*-type material, Te satisfies these criteria and has been found to transport with near unity efficiency. Ge has a higher diffusion coefficient, although it was also found to be a suitable dopant. Si doping was also investigated, but the oxides are not volatile and transport is negligible. Other dopants were not intentionally added, though we have found traces of sulfur acting as an unintentional *n*-type dopant in nearly all of our depositions.

There are few suitable *p*-type dopants available for an H_2O-CSVT reactor. Beryllium was not chosen due to the low vapor pressure of the elemental form and oxide. Mg has a high vapor pressure, but has a high affinity for oxygen and its oxides have a low vapor pressure. Hg has reportedly low incorporation in MBE due to its high volatility even at low temperatures and would be undesirable due to its low melting point. Carbon is not volatile at accessible growth temperatures. Thus, Zn and Cd were chosen as dopants for this study.[42]

We had previously shown that CSVT can be used to deposit thin films of *n*-GaAs and *p*-GaAs with minority carrier diffusion lengths (L_D) of >1 μm and photovoltages equivalent to those of MOCVD-grown GaAs films when measured in non-aqueous photoelectrochemical (PEC) cells.[43,44] Our previous studies use single-crystal GaAs wafers as the source material. Powder sources are potentially less expensive than single-crystal sources and also present a simple way to introduce dopants. We weighed and added impurities to the powdered GaAs sources (i.e. Zn, CdAs, and Te) and grew GaAs films from them. We measured their dopant and free carrier concentrations using SIMS (Figure 2) and a combination of impedance spectroscopy and Hall effect measurements (Table 1).

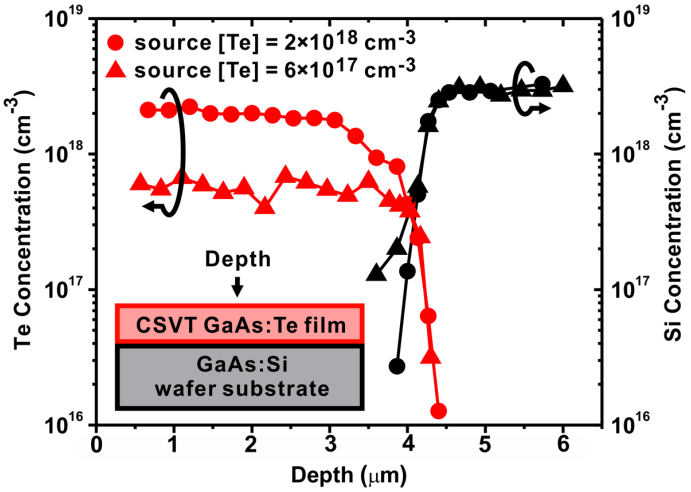

Figure 2: SIMS depth profiles of two *n*-GaAs films grown from differently-doped GaAs:Te sources on GaAs:Si substrates. The Te depth profiles are shown in red and Si in black. Circles denote the film was grown from a source containing [Te] = 2 × 10^{18} cm^{-3}, triangles denote the film was grown from a source with [Te] = 6 × 10^{17} cm^{-3}.

CSVT using doped GaAs powder sources yielded films with the same free electron concentration (N_D-N_A) as those grown from equivalently-doped GaAs wafers. Te transports with unity efficiency while Zn transports with ~1% efficiency (Table 1). We attempted Cd doping by adding CdAs powder to GaAs powder at [Cd] = 10^{18} cm^{-3} but found that the material appeared to be heavily compensated. Our initial explanation for this was that the Cd may have incorporated as an electrically-inactive defect center. However, in later experiments the unintentional *n*-type background was found to be as high as ~10^{18} cm^{-3} and was eventually traced to contamination of both the graphite heaters and the quartz reactor tube. By that time, however, Zn was found to be adequate for the purposes of demonstrating control of *p*-type doping and *pn* junctions so further experiments with Cd were not carried out.

Table 1 Dopant densities (measured by impedance analysis and Hall Effect) and impurity concentrations (determined by TOF-SIMS analysis) of several CSVT GaAs films deposited from powder and wafer sources.

powder or wafer source	source dopant species (E)	source [E] (cm^{-3})*[a]	Impedance analysis N_D-N_A (cm^{-3}) (average of three electrodes)	Hall Effect N_D-N_A (cm^{-3}) (one sample)	[E] from SIMS (cm^{-3}) (one sample)
wafer	Te	2-4 × 10^{18}	3×10^{18} ± 1×10^{18}	--	2×10^{18}
powder	Te	2-4 × 10^{18}	4×10^{18} ± 1×10^{18}	3×10^{18}	--
wafer	Te	3-6 × 10^{17}	4×10^{17} ± 4×10^{16}	3×10^{17}	6×10^{17}
powder	Te	3-6 × 10^{17}	7×10^{17} ± 2×10^{17}	6×10^{17}	--
powder	Zn	5 × 10^{21}	-2×10^{19} ± 3×10^{18}	-4×10^{19}	--
powder	Zn	5 × 10^{20}	-4×10^{18} ± 7×10^{17}	-4×10^{18}	--
wafer	Zn	1-2 × 10^{19}	-2×10^{17} ± 1×10^{16}	-1×10^{17}	1×10^{17}
powder	S†[b]	-†[b]	1×10^{17} ± 4×10^{16}	2×10^{16}	3×10^{16}
wafer	S†[b]	-†[b]	7×10^{16} ± 3×10^{16}	8×10^{16}	7×10^{16}

*[a]: for wafer sources the dopant density was provided by the manufacturer; for Zn-doped powder sources the dopant density was calculated from the mass of the GaAs powder and the Zn powder used. †[b]: the S dopant was not intentionally added.

As N_D and N_A are increased, μ_e and μ_h decrease due to increased scattering from the ionized dopant atoms in the lattice (Figure 3).[42,45,46] The measured μ_e and μ_h of CSVT GaAs films deviate from the MOCVD values more for lightly-doped samples than for highly-doped samples. This is likely because at lower N_D or N_A, the influence of trace compensating impurities and crystal defects becomes important relative to the dopant atom scattering. Overall, these results indicate that CSVT from GaAs powder sources is competitive with MOCVD in terms of the achievable μ_e and μ_h for a wide range of N_D and N_A.

No significant differences were observed between films deposited from powder and wafer sources. This result is expected because the growth takes place at the interface between substrate and the gas phase. Thus the source's crystalline quality should not affect the CSVT process as long as it does not affect the ability of the surface to be etched by H_2O to produce vapor phase As_2 and Ga_2O. This implies that there is no need for crystalline powder sources, and lower quality powders could potentially be used as sources, for example those made by reaction of Ga and As at low temperatures.[47]

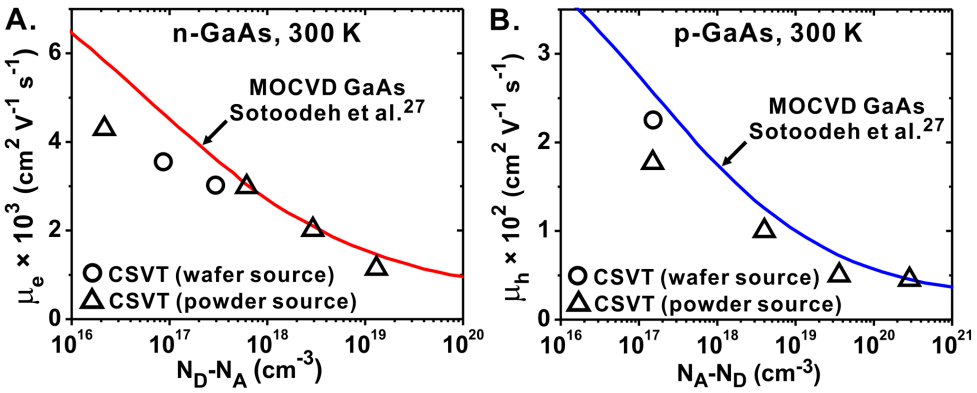

Figure 3: Hall mobilities of *n*- and *p*-GaAs films as a function of N_D and N_A. Solid curves represent the Hall mobility of high-quality epitaxially-grown MOCVD GaAs.[48]

PEC Characterization (Subtask 1.2)

The PEC GaAs|electrolyte junction is a convenient tool which enables the study of material properties such as photocurrent *vs* potential (*J-E*) response, impedance spectroscopy, and Φ_{int} without fabrication of solid state devices.[44,49,50] Electrodes of CSVT *n*-GaAs films were immersed in a non-aqueous ferrocene/ferrocenium electrolyte (Fc/Fc^+) and their *J-E* response was measured under 100 mW cm^{-2} of simulated AM1.5G irradiation.[50] Commercial <100>-oriented single-crystal wafers were measured as controls. The CSVT samples produced open-circuit voltages (V_{oc}) up to 0.83 V, equivalent to that attained by others using MOCVD *n*-GaAs.[51,52] Short-circuit current density (J_{sc}) was ~20 mA cm^{-2} for moderately-doped samples having N_D = 10^{16} ~ 10^{17} cm^{-3}. The performance of all samples exceed the bare substrates and similarly-doped GaAs control wafers (Figure 4A). There were no significant differences between films grown from powder and wafer sources. Lower photocurrent was observed in

highly-doped samples, due to the reduced μ_h (and consequently L_D).[42,46]

Electrodes of CSVT *p*-GaAs films and control wafers were immersed in an aq. iodide/triiodide electrolyte (I^-/I_3^-) and their *J-E* response was measured under 100 mW cm^{-2} of simulated AM1.5G irradiation (Figure 4B).[53,54] The V_{oc} was 0.15 - 0.20 V *vs* E_{sol}, lower than the *n*-GaAs samples due to surface pinning of the *p*-GaAs Fermi level near the valence band edge.[53] The best samples exhibited J_{sc} ~20 mA cm^{-2}, similar to the best *n*-GaAs samples despite the higher parasitic light absorption of the I^-/I^{3-} electrolyte. All CSVT *p*-GaAs films (including those synthesized with $N_A > 10^{18}$ cm^{-3}) exhibited higher photocurrent than the *p*-GaAs control wafer ($N_A = 1\times10^{18}$ cm^{-3}, J_{sc} = 12 mA cm^{-2}) indicating lower bulk recombination and a longer L_D.

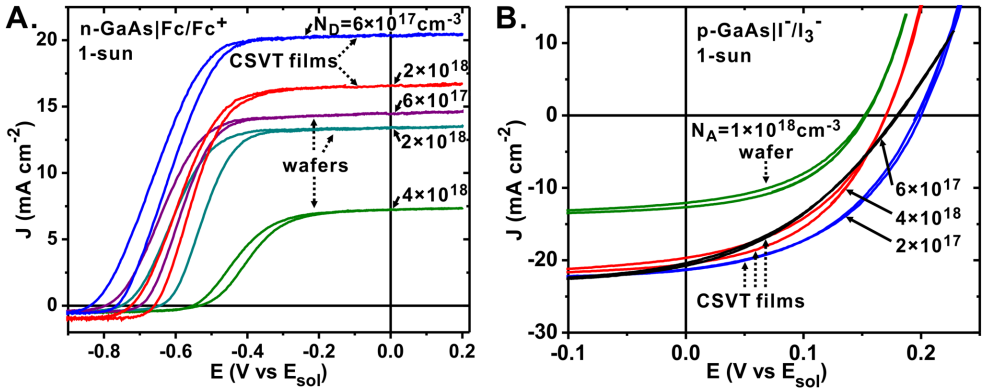

Figure 4: Photoelectrochemical *J-E* curves of (A) *n*-GaAs and (B) *p*-GaAs CSVT films and control wafers. The curves are labeled with the corresponding sample's free carrier concentration in cm^{-3}. The selected curves are representative of other electrodes obtained from the same samples and from other samples with similar free carrier concentrations.

In order to determine the L_D for each sample we measured the spectral response using the short-circuit PEC configuration (E_{WE} = 0 V *vs* E_{sol}) under low-intensity chopped monochromatic light. For the *n*-GaAs films such measurements in the Fc/Fc^+ electrolyte are well-developed. Spectral response measurements of *p*-GaAs in aqueous I^-/I^{3-}, however, were complicated by the solubility of GaAs in the acidic I^-/I^{3-} electrolyte.

No etching of *p*-GaAs was observed in the aq. solution after hours of sustained operation as long as illumination was provided. However, a nA-range anodic current was observed in the aqueous solution when under dark or low-light conditions (< 1 μW cm^{-2}). This was problematic for spectral response, (which uses a nA-range chopped light source) and impedance analysis, which is conducted in the dark. We suspect the *p*-GaAs surface, while unstable in H_2O especially at low pH,[55] is cathodically stabilized by the photo-excited minority carrier electrons, causing it to act as a photo-gated battery.

Therefore we used a non-aqueous solution for the *p*-GaAs spectral response and impedance measurements. We used NaI to provide I^- rather than HI. We also reduced the concentration of redox couple in order to decrease parasitic light absorbance. The low-concentration of redox couple in non-aqueous solution was sufficient to support the nA-range signal and exhibited no photo-gated current.

Trends for both *n* and *p*-type GaAs in J_{sc} were mirrored by the spectral response curves (Figure 5). Due to the wavelength dependence of $\alpha(\lambda)$, photons with energies near the band-gap E_g are absorbed further from the surface than those with higher energies. Thus Φ_{int} decays to zero at E_g. This can be modeled using the Gärtner equation, which assumes no depletion region recombination and that the L_D governs bulk recombination:

$$\Phi_{int} = \left(1 - \frac{e^{-\alpha(\lambda)W}}{1+\alpha(\lambda)L_D}\right) \quad (1)$$

where W is the width of the semiconductor depletion region.[56] This approach produces reliable estimates of L_D for GaAs[52] and other semiconductors.[57] Using this technique we measured three electrodes of each film.

One parameter fits to Φ_{int} from eqn. (5) match the experimental data well (Figure 5). Moderately-doped *n*-GaAs CSVT films have L_D ~ 2.9 ± 0.2 μm, while CSVT p^+-GaAs films possess L_D = 5.4 ± 0.1 μm and moderately-doped *p*-GaAs films possess L_D = 7.4 ± 0.4 μm. The L_D is higher in *p*-GaAs because μ_e is higher than μ_h, which in turn is due to the curvature of the conduction and valence bands.[58] For all CSVT samples, the measured L_D was significantly higher than that of the control GaAs wafers (L_D = 0.42 μm for *n*-GaAs:Te, 0.16 μm for n^+-GaAs:Si, 0.45 μm for *p*-GaAs:Zn, and 0.05 μm for p^+-GaAs:Zn) and consistent with one-sun J_{sc} measurements (see above).

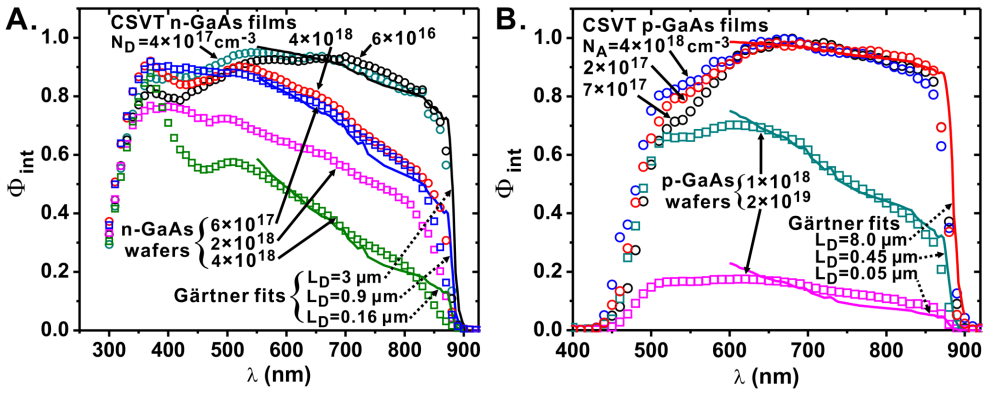

Figure 5: Φ_{int} measurements obtained using PEC on *n*-GaAs (A) and *p*-GaAs samples (B). Experimental data is plotted as circles and calculated L_D fits from eqn. (5) are plotted as solid curves. The selected curves are representative of other electrodes obtained from the same samples and from other samples with similar free carrier concentrations.

Electron-beam induced current (EBIC) Studies (Subtask 1.3)

We conducted EBIC measurements on CSVT *n*-GaAs films to supplement the L_D obtained from spectral response measurements. The spectral response L_D is calculated by fitting a curve of internal quantum efficiency (Φ_{int}) vs. optical excitation wavelength (λ), which decays as the absorption coefficient $\alpha(\lambda)$ decreases according to Gärtner's equation. Determination of Φ_{int} by this method therefore requires that some photons be absorbed at a depth greater than $L_D + W$ so that there will be some decay to be fit. However, since α(λ) for GaAs is large, when L_D exceeds 2~3 μm the fraction of photons absorbed deeper than $L_D + W$ is small and there is little decay to fit (Figure 6).

In EBIC analysis the proximity of the excitation source to the charge separating junction is controlled by rastering an electron beam away from a metal Schottky contact (Figure 6), and is thus independent of $\alpha(\lambda)$. The relationship of the current decay to L_D is given by the relation:

$$I = qN_C e^{-X/L_D} \quad (2)$$

Where I is the beam-induced current, N_C is the number of minority carriers generated by the excitation beam per second, and X is the separation between the excitation volume and the rectifying junction.[59]

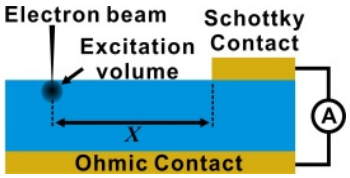

Figure 6: Schematic drawing of the EBIC experiment setup.

In addition to the required ohmic and rectifying contacts, two additional conditions must be satisfied for EBIC measurements to be accurate. First, the current decay must be dominated by bulk recombination. Second, the excitation volume (which depends on the accelerating voltage used) must be small with respect to L_D. For unpassivated GaAs, the EBIC decay is dominated by the high (34,000 cm s^{-1}) surface recombination velocity (SRV) rather than bulk recombination when accelerating voltages < 10 keV are used. When larger accelerating voltages are used (>15 keV), the excitation volume becomes large with respect to L_D and the measured decay leads to erroneously high values of L_D (Figure 7A). We found that GaAs surface passivation by Na_2S (SRV = 5,500 cm s^{-1})[60] was sufficient to allow measurement of L_D even for small excitation volumes (Figure 7B).

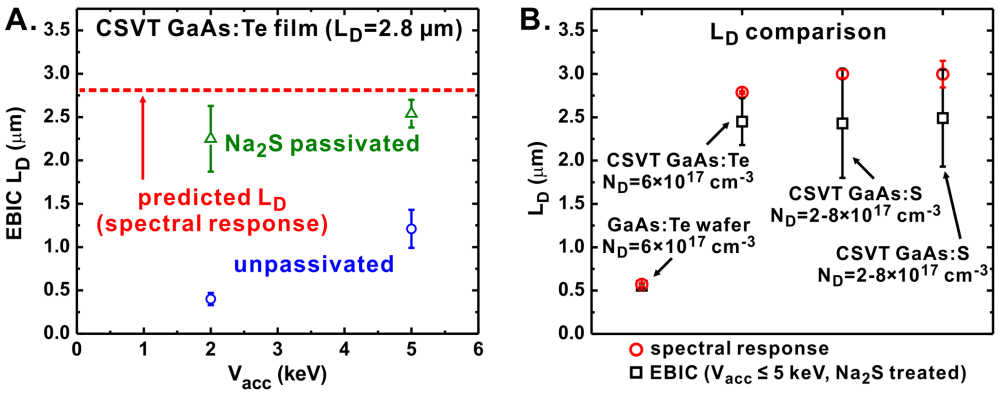

Figure 7: (A) L_D measured by EBIC on the same CSVT GaAs film before and after passivation by Na_2S. The dashed line indicates the L_D predicted by spectral response. (B) Comparison of L_D obtained by spectral response and EBIC techniques.

The L_D measured by EBIC on Na_2S-passivated GaAs using low (2-5 keV) accelerating voltages was similar to the L_D obtained from spectral response

measurement (Figure 5). We note that EBIC generally yielded a larger range of L_D's than the spectral response technique. We believe this is caused by microscopic defects in the GaAs. Such defects could greatly affect the signal detected by the EBIC technique (which measures the current from a 1-D linescan), while with spectral response the photocurrent is collected from an area ~0.03 cm^2 and small defects simply become part of the average signal.

Milestone (Subtask 1.3): Demonstrate films with p-type doping from 10^{17} cm^{-3} to 10^{19} cm^{-3} and L_D > 2 μm

We used a combination of Hall effect, PEC, and EBIC measurements to characterize carrier concentrations, majority carrier mobilities, and minority carrier diffusion lengths in both *n*- and *p*-type films. Doping with Zn was achieved over a range of 10^{17} – 10^{19} cm^{-3} by changing the source composition. CSVT films have higher J_{sc} in PEC test cells as compared to comparably-doped wafers, and spectral response measurements of these cells give diffusion lengths exceeding 7 μm for *p*-type films.

Task 2. Fabricate, test, and optimize epitaxial pn junction devices

Device architecture and simulations (Subtask 2.1)

We considered both n^+p and p^+n device architectures, but chose the former due to the higher minority carrier diffusion lengths found for *p*-type layers as described above. Simulations of such structures using PC1D showed that efficiencies could reach ~25% efficiency given the measured L_D and estimates for minority carrier mobility. Without surface passivation, efficiencies are limited (see Figure 8) as untreated GaAs surfaces have surface recombination velocities ~10^6 cm s^{-1}.[61] Later simulations were performed using SCAPS software and produced results consistent with PC1D.

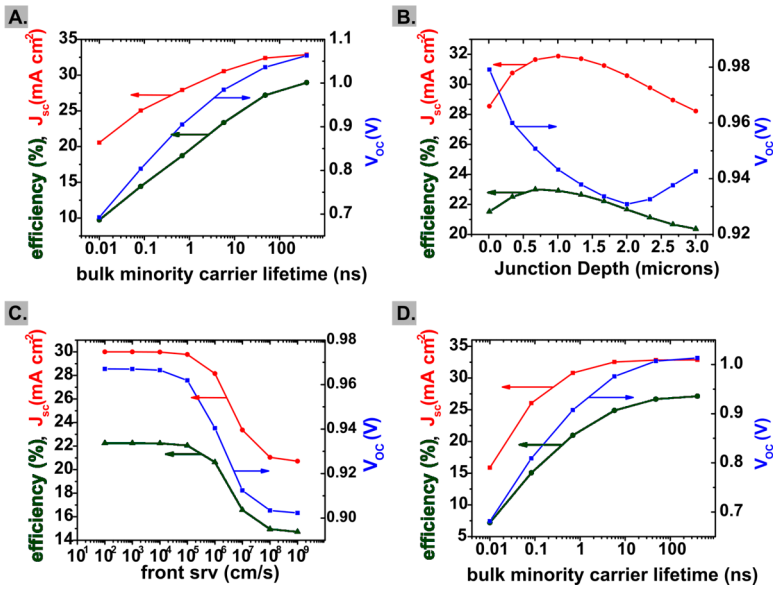

Figure 8: Simulations of p^+n devices using PC1D.

Initial optimization of emitter growth parameters (Subtask 2.2 and 2.3)

Initial devices were n^+ CSVT-grown films with moderately-doped (~5×10^{17} cm^{-3}) *p*-type wafers serving as the substrate and absorber film. The first devices had V_{oc} < 500 mV and J_{sc} < 8 mA/cm^2, were all grown from Te-doped wafers, and had rough surface morphologies. V_{oc} is chosen as the primary figure of merit for our devices since it does not depend strongly on details such as emitter thickness, contact resistivity, or surface recombination. Thus we expect V_{oc} to be a good measure of junction quality as well as bulk absorber quality.

Higher V_{oc} was obtained by using a powder source produced by grinding undoped pieces of GaAs wafer together with an appropriate weight of Te powder to dope the powder to 10^{19} cm^{-3}. This powder was then pressed into a pellet to produce an approximately planar source that could be conveniently loaded into the CSVT reactor. A Ge-doped pellet was prepared using the same method. Annealing in an evacuated quartz ampoule was necessary to diffuse Te throughout the pellets due to the high vapor pressure of metallic Te. Films grown from pellet sources are consistently specular, though surface defects are usually observed on the surfaces. Films grown from sources doped with greater than about 10^{19} cm^{-3} Te atoms exhibited surface defects which were elongated in the (110) direction (a comparison is shown in Figure 9). This is likely due to a surfactant effect of Te, which changes the adatom diffusion kinetics, and the relatively smooth profile of these defects may be responsible for the high V_{oc} of these devices. Surface morphology is further discussed in subsequent sections.

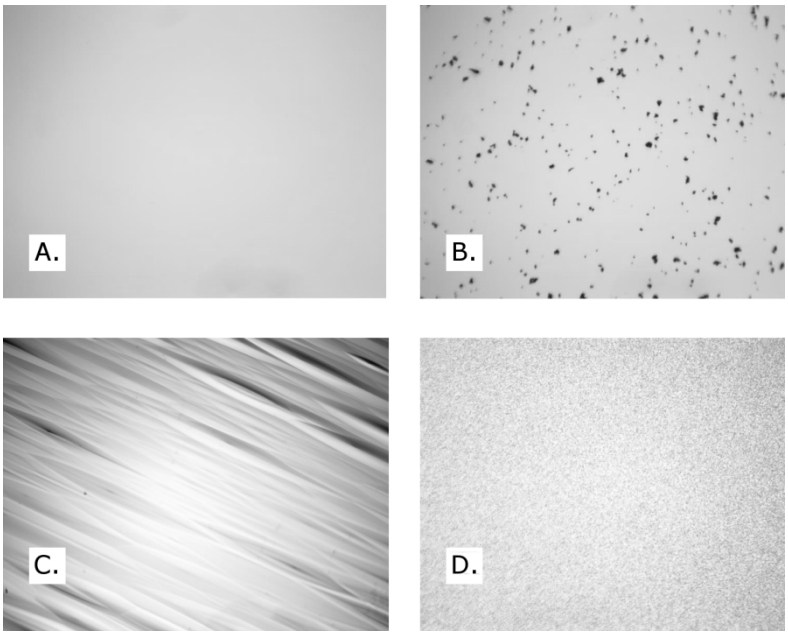

Figure 9: Optical microscope images of **A)** clean wafer surface **B)** surface after deposition of film from a powder source showing large density of surface defects **C)** surface after deposition from a highly Te-doped pellet showing elongated oval hillock defects **D)** rough surface after deposition from a wafer source.

With one exception, the substrate for all of these emitter films was a *p*-type wafer doped with Zn to ~10^{17} cm^{-3}. The other film was grown on a piece of a *p*-type CSVT film which was later confirmed by SIMS to be doped with Zn to 10^{17} cm^{-3} and was known to have a very long electron diffusion length. Various growth temperatures were explored to determine the effect of diffusion of Zn from the substrate, and it was found that device performance did not correlate to growth temperature up to 850 °C, but J_{sc} was strongly correlated to emitter thickness. Current-voltage curves are shown in Table 2 for devices using emitters grown from highly doped sources.

Table 1: IV characteristics for a series of n^+p devices with standard deviations of device characteristics given as uncertainties. Film 4 is an emitter grown on a CSVT film, while the others are grown on commercial wafer substrates.

Film	Source doping	T_{src} (ºC)	T_{sub} (ºC)	V_{oc} (mV)	J_{sc} (mA/cm^2)	Eff. (%)	FF (%)
1	Te 10^{19} cm^{-3}	850	830	846 ± 44	7.9 ± 0.6	4.8 ± 0.7	72 ± 7
2	Te 10^{19} cm^{-3}	850	830	872 ± 8	8.5 ± 0.4	5.5 ± 0.1	75 ± 2
3	Ge 10^{19} cm^{-3}	850	830	402 ± 91	5.7 ± 0.6	1.3 ± 0.2	60 ± 8
4*	Ge 10^{19} cm^{-3}	850	830	320 ± 153	6.9 ± 1.3	1.1 ± 0.6	46 ± 7
5	Te 10^{19} cm^{-3}	760	720	834 ± 42	12.3 ± 0.2	7.1 ± 0.7	69 ± 4
6	Te 10^{19} cm^{-3}	780	720	868 ± 35	8.3 ± 0.8	4.8 ± 1.9	64 ± 23
7	Te 10^{19} cm^{-3}	800	740	863 ± 35	11.9 ± 0.5	7.6 ± 0.4	74 ± 2
8	Te 10^{19} cm^{-3}	820	760	783 ± 20	10.7 ± 0.8	5.7 ± 0.4	68 ± 1

The highest efficiency achieved was 8.1 % for one device on film 7. The corresponding dark and simulated 1-sun illuminated IV curves are shown in Figure 10. Quantum efficiency measurements on these devices suggested that photocurrent could be improved by further tuning the emitter doping and thickness as well as using CSVT absorber layers which have higher electron diffusion lengths based on PEC measurements.

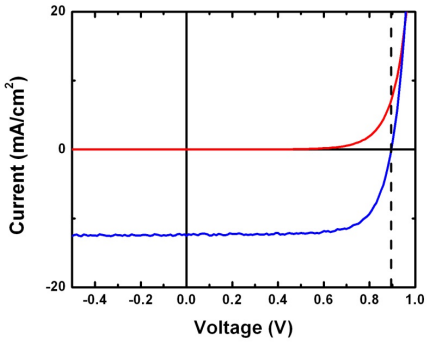

Figure 10: Light and dark IV curves for the 8.1% efficiency device from film 7.

Initial CSVT absorber results (Subtask 2.2)

We found that the devices fabricated from a CSVT absorber film had a QE response which peaked very near the band edge (Figure 11). This indicated that much of the light was absorbed by the emitter and was not contributing to photocurrent. Since the PEC QE measurement of the absorber had a larger peak value, we expected that this device should have a better response if the emitter was thinner. Chemically etching

the emitter in several steps improved Φ_{int} significantly. Collection from carriers excited by 300-400 nm light is still limited, but this is expected for an unpassivated device as this light is absorbed near the front of the cell where surface recombination is dominant.

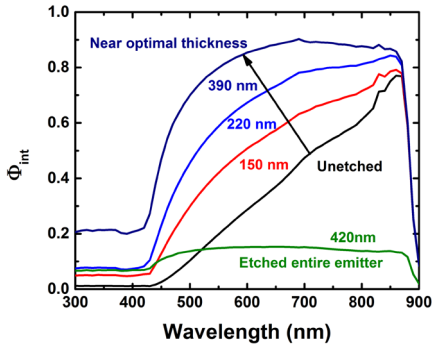

Figure 11: Φ_{int} at various etch depths of the device from film 4 with both emitter and absorber grown by CSVT.

Time-of-flight secondary ion mass spectrometry (TOF-SIMS) has been useful in characterizing dopant concentrations and potential contaminants. For most elements of interest, the TOF-SIMS available at the University of Oregon has a high enough sensitivity; however, profiles of Zn at a level of 10^{17} cm^{-3} require a magnetic sector SIMS. Due to the expense, only the *pn* junction device described above has been profiled for Zn concentration (Figure 12). The result shows that at a high growth temperature (830 ºC substrate) both Zn and Ge drop by a factor of 10 to below the detection limit in only ~100 nm, which suggests that Zn diffusion during emitter deposition is minimal. The abruptness of the junction can be further improved as emitters have been deposited at substrate temperatures as low as 760 °C without substantial degradation in film quality. The level of compensation by *n*-type dopants can be found by comparing SIMS results with carrier concentrations found by capacitance-voltage profiling of the devices, and suggests a compensation of 6×10^{16} cm^{-3}. This is consistent with the background sulfur levels found in films grown as part of the same series.

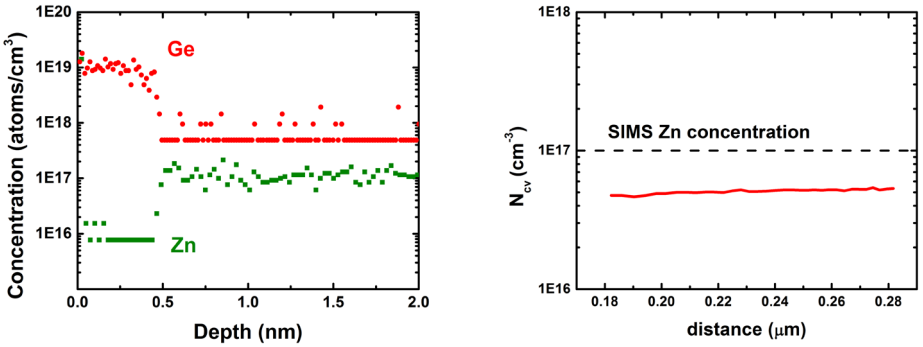

Figure 12: SIMS data from QSpec Technology (left) for device with both emitter and absorber grown by CSVT and capacitance-voltage profile (right) for a different device on the same film.

Device reproducibility (Subtask 2.3)

One issue affecting the reproducibly of CSVT devices is the necessity of maintaining a clean reactor environment with low background doping. We had intermittent issues with background doping that required addressing. For example, two Hall effect samples on semi-insulating substrates were prepared which were grown interspersed with *p*-type absorber films that were later process into pn junction devices. Of these, one exhibited an *n*-type response and one exhibited a *p*-type response with a doping of only 4 × 10^{15} cm^{-3} though the expected doping was ~1 × 10^{17} cm^{-3}. Capacitance-voltage measurements of the devices also yielded carrier densities ~10^{15} cm^{-3}. Subsequently, unintentionally doped films were grown and characterized by Hall effect to determine an *n*-type background doping of 2-3 × 10^{17} cm^{-3}.

A series of control experiments were performed to determine a suitable cleaning procedure for the reactor to return background levels to ~10^{16} cm^{-3}. It was found that cleaning the graphite heaters by soaking in a solution of 3:1 $HCl:HNO_3$ had negligible impact on background dopant levels. Ultimately, background levels were reduced by replacing the quartz reactor tube, and intermittent cleaning in 6:1:1 $H_2O:HCl:H_2O_2$ has been adopted to keep background levels low. These results suggest that the quartz tube can accumulate adventitious sulfur from the atmosphere during sample changing, for example.

Investigation of surface defects (Subtask 2.3)

A careful survey of film surfaces using Nomarski interference microscopy shows there are several types of defects which may occur in our CSVT GaAs films. Those with irregular shapes most often appear in the first growth from a pellet, and may be the result of particulate transfer from pressed powder source material onto the substrate. In some cases, polyhedral pits are observed and these were eliminated by replacing the isopropanol and H_2O used for rinsing the surface prior to growth. Other surface defects have a circular (at lower growth temperatures) or oval aspect and also appear to originate from surface contamination of the substrate prior to growth as they are present in even the thinnest films.

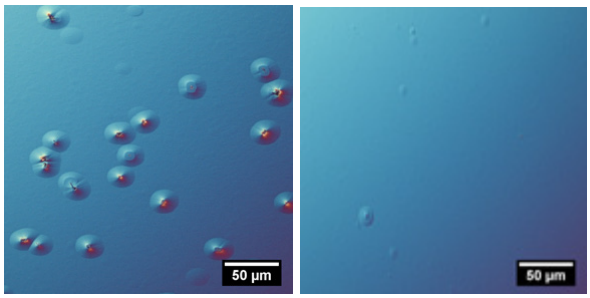

Figure 13: Nomarski interference images of emitter films without (left) and with (right) pre-growth annealing.

Huang et al. previously reported similar defect structures in CSVT GaAs, but they were unable to change the density of surface defects on non-miscut substrates.[62] In one trial, we found that a 5 minute anneal under H_2 (with [H_2O] ~ 100 ppm) at 780 °C significantly improved the surface morphology of CSVT films grown on non-miscut wafers. This was not reproduced when a new Zn-doped pellet was used to grow thick films on wafers cleaved from the same ingot.

N-type films shown in Figure 13 were deposited on a *p*-type wafer with N_A = 5 × 10^{17} cm^{-3} and were subsequently processed into devices to explore the impact of emitter surface morphology on device performance. The film with pre-growth annealing exhibited much less scatter in its IV curves. V_{oc} has also been shown to decrease with

increasing surface density for devices with CSVT absorbers as shown in Figure 14. The defect density was estimated using ImageJ software to analyze Nomarski micrographs.

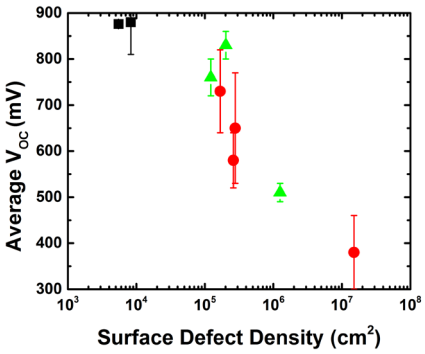

Figure 14: Average open-circuit voltage decreases with increasing absorber surface morphological defect density. Colors and marker shape indicate absorber films grown from different source pellets. Error bars show the standard deviation of the value for the 10 mesas fabricated from each *pn* junction. The data constitutes ~100 individual *pn* junction devices.

Oval hillocks are reported in MBE,[63–65] CSVT,[62] and less commonly MOCVD vapor growth of GaAs. In MBE, they are often associated with the Ga source, either due to Ga droplets or cubic Ga_2O_3 phases which cause stacking faults in the epitaxial films.[66] Particulates or other foreign contaminants may be a separate cause of morphological defect formation, or may provide nucleation sites for Ga clusters or oxides. In the latter case, using a halide transport agent may decrease the density of surface defects even without reducing substrate contamination as all of the oxides could be etched away in-situ prior to growth.

Ultimately, our best devices are those with few surface defects. The record device shown in (Figure 15) has J_{sc} = 13.9 mA/cm^2, V_{oc} = 914 mV and efficiency of 9.5 %. This is similar to the current best published HVPE cell with similar structure (no surface passivation) and J_{sc} = 11.8 mA/cm^2 and V_{oc} = 936 mV.[67]

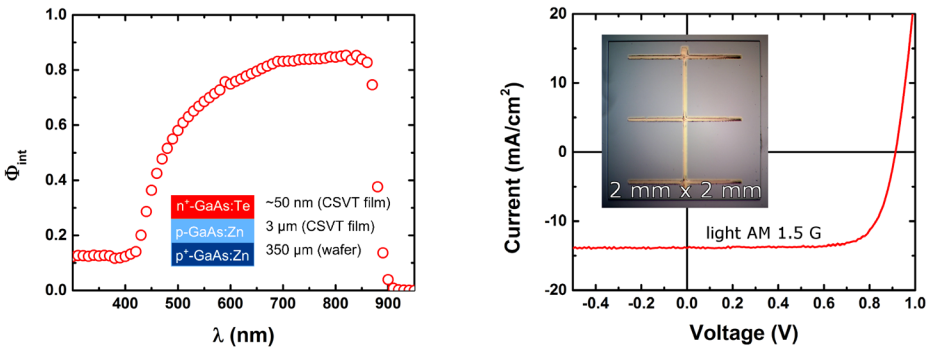

Figure 15: Left: JV curve for record efficiency device under 1-sun simulated illumination. Right: Internal quantum efficiency for the same device.

Electrical characterization of pn junction devices (Subtask 2.3)

The deep defect levels which are common in GaAs have been well-established for material grown by melt techniques, MBE, and MOCVD. Low-cost alternative techniques

such as CSVT and HVPE have not been as extensively characterized. We have performed a preliminary comparison of the defects present in both our CSVT devices and devices made by the aforementioned techniques from collaborators at NREL and Microlink Devices.

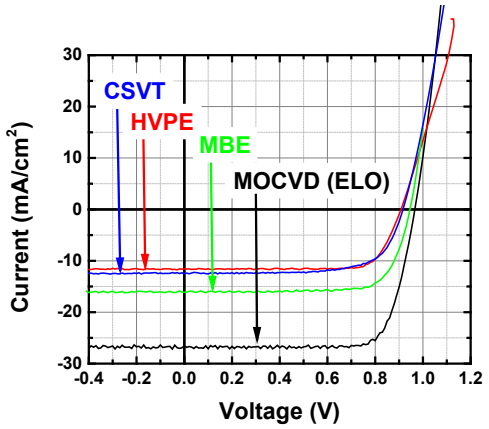

Figure 16: IV comparison of devices chosen for TPC/TPI study.

Transient photocapacitance and photocurrent spectroscopy (TPC and TPI) was originally developed to investigate optical transitions amorphous silicon solar cells.[68] Although crystalline GaAs is a much simpler system for study, there is no published TPC or TPI data in existence for III-V materials. The devices we tested were chosen such that they all had V_{oc} > 900 mV (Figure 16) indicating moderate to good quality for the absorbing material and interface. The MOCVD cell was an epitaxial liftoff (ELO) device and also included surface passivation and antireflective coating.

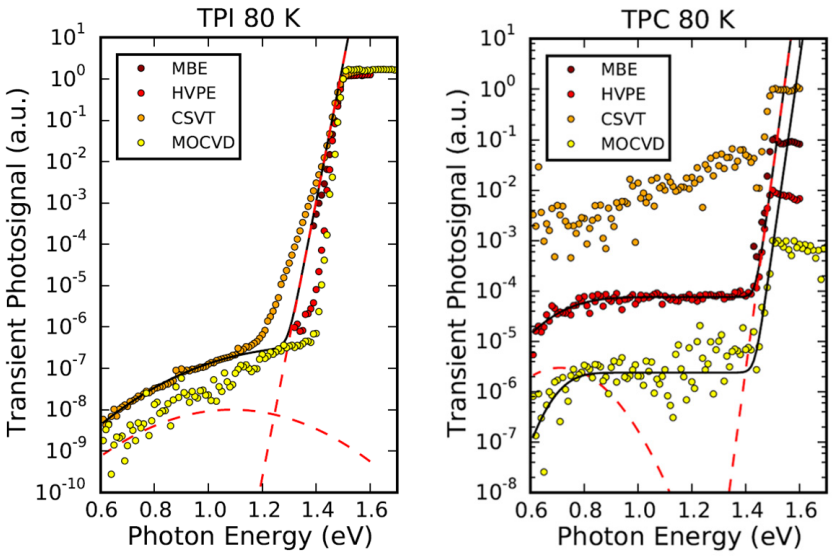

Figure 17: TPI and TPC spectra collected at 80 K for the four cells and corresponding fits. Some spectra were not fit since they did not fit the model of a single Gaussian distribution for the defect band.

An interesting feature is the band edge broadening visible in the CSVT TPI spectrum, which can be attributed either to the substrate itself or the interface with the substrate (Figure 17). This does not appear in TPC due to a different spatial sensitivity for carrier collection. A comparison of TPC and TPI may therefore be useful in characterizing the effect of epitaxial liftoff techniques since it can separate response near the junction from response deeper in the device. It is difficult to draw any further conclusions from such a small sample set in regards to the differences between the growth techniques, though it is worth noting that there are at least two Gaussian defect bands detected in the CSVT device in contrast to the MOCVD and HVPE device. This

could be due simply to the fact that the CSVT reactor is not as highly engineered and has more possible contamination sources.

Task 3: Develop transport conditions for $GaAs_{1-x}P_x$ deposition and optimize properties

Varied composition growths (Subtask 3.1)

Following the standard set for dopant incorporation during **Task 1**, powder sources of $GaAs_{1-x}P_x$ were produced from single crystal GaAs and GaP wafers. The transport process for a mixed powder source is expected to proceed as follows:[34,69]

Source: $2(GaAs)_{1-x}(s) + 2(GaP)_x(s) + H_2O(g) \rightleftharpoons Ga_2O(g) + H_2(g) + (As_2)_{1-x}(g) + (P_2)_x(g)$

Substrate: $Ga_2O(g) + H_2(g) + (As_2)_{1-x}(g) + (P_2)_x(g) \rightleftharpoons 2GaAs_{1-x}P_x(s) + H_2O(g)$

In order to explore the available range of compositions and gauge the effect of source composition on final film composition, five powder sources were produced with 0.3 < [P] < 0.7. To eliminate transport conditions as a confounding factor, a single set of growth parameters was used for this composition series (T_{src} = 900 °C, ΔT = 20 °C, [H_2O] ~2500 ppm, t = 20 min).[38]

Film compositions were determined using both x-ray diffraction (XRD) and energy dispersive spectroscopy (EDS) and compared to the source compositions (Figure 18). P incorporation was high over the entire composition range, with an average 10% reduction in P from source to film across the series. This is an improvement over MOCVD and MBE, which require a large excess of precursors (3x for group III and >10x for group V species)[70] or group V precursor cracking, respectively.[71,72] The reduction in [P] from source to film can be attributed to the loss of the precursor from the growth zone, which is not completely enclosed, and due to the higher diffusivity of P_2 than As_2 due to its smaller size.

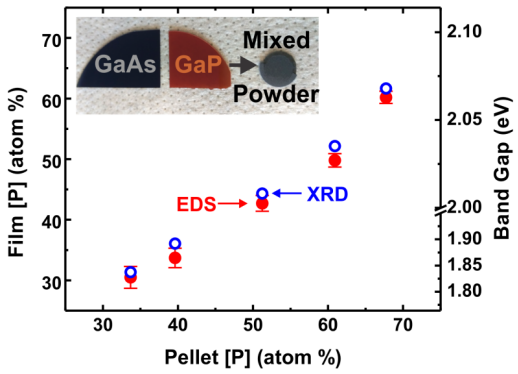

Figure 18: The pellet source and film compositions of the varied composition $GaAs_{1-x}P_x$ films. The second y axis shows expected E_g based on [P]. Images of the source wafers and a pellet are inset.

High-resolution coupled ω-2θ XRD scans confirmed that the films were epitaxial, aligned to the <100> GaAs surface. These measurements were also used to gauge the crystalline quality of the composition series films. Rocking-curve measurements of the $GaAs_{1-x}P_x$ (004) peak gave full-width half-maximum (FWHM) values which were compared to the GaAs substrate FWHM (Figure 19A). As expected due to the smaller

lattice parameter for all $GaAs_{1-x}P_x$ compositions, all films showed a larger FWHM than the substrate as a result of misfit dislocations originating at the interface. Measurements across the *2θ* range showed increasing [P] across the series, as the $GaAs_{1-x}P_x$ (004) diffraction peak shifts away from the substrate (004) (Figure 19). Some minor compositional inhomogeneity is evident in all of these samples except for [P] = 31%, based on the small lower-angle shoulder on each $GaAs_{1-x}P_x$ (004) peak.

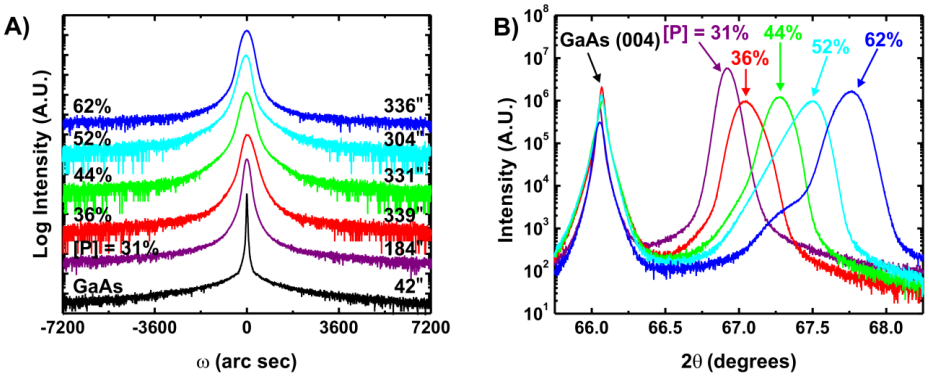

Figure 19: A) Rocking curve (*ω*) scans of each $GaAs_{1-x}P_x$ (004) peak for the varied composition samples. FWHM values of all films are large compared to the GaAs substrate, a result of misfit dislocations. **B)** θ/2θ scans of the same samples, showing the shifting $GaAs_{1-x}P_x$ (004) peak with increasing [P].

Varied temperature growths (Subtask 3.1)

After the composition series established that the entire range of [P] could be accessed using CSVT, a single composition was chosen for exploration of the effect of growth temperature on the $GaAs_{1-x}P_x$ films grown by this method. $GaAs_{0.7}P_{0.3}$ was chosen for this portion of the study because $E_g \approx 1.7$-1.8 eV, ideal for integration into a Si-based heterojunction device as envisioned in **Task 4**.[73] Ten $GaAs_{0.7}P_{0.3}$ films were grown consecutively at various T_{src} from a single [P] = 30% pellet, allowing for monitoring of the source material as well as resulting film quality and [P] incorporation. T_{src} varied between 800 and 950 °C while ΔT was held constant at 20 °C (i.e. for T_{src} = 900 °C, T_{sub} = 880 °C). Data for this series can be seen in Table 4.

Table 2: **Temperature series film data**

Sample	T_{src} (°C)	Film [P] by XRD (atom %)	Difference from source (%)	Film Thickness (μm)
T1	900	30.2	2.3	4.9 ± 0.7
T2	950	25.5	13.4	8.7 ± 1.6
T3	900	26.8	9.3	4.4 ± 0.4
T4	850	27.9	5.4	1.9 ± 0.2
T5	900	26.0	11.8	3.8 ± 0.5
T6	800	27.4	7.0	1.2 ± 0.5
T7	900	27.7	6.2	4.1 ± 0.3
T8	900	28.1	4.5	3.8 ± 0.6
T9	900	27.5	6.7	4.2 ± 1.0
T10	900	27.7	6.1	4.4 ± 0.6

Monitoring the composition of the source is especially important for the commercial viability of CSVT, as the depletion of one group V element (anticipated in this case to be phosphorous, given the reduction in [P] observed in the films of the

composition series) would cause film compositions and therefore E_g to drift from their targets. The composition of the pellet was qualitatively monitored using x-ray fluorescence (XRF) and measured before every growth following a short 800 °C pre-anneal under H_2 to improve its mechanical stability. The evolving pellet composition was then compared with the composition (based on XRD) of the films which were grown at different temperatures.

The first growth caused a significant depletion of P from the pellet, possibly leading to the significantly higher P content of that film than the others in the series (Figure 20A). This sample also shows compositional inhomogeneity which is not displayed by other films in the series (Figure 20B).These results suggest sintering at 900 °C may be sufficient to drive the alloying of GaAs and GaP in the source material and that compositional inhomogeneity of the partially sintered pellet contributed to the low crystalline quality of the first sample, which also has a much higher FWHM than other $GaAs_{0.7}P_{0.3}$ films grown using the same conditions (Figure 20C). The other FWHM values follow the trend set by film thicknesses as seen in Table 4, with the highest growth temperature producing the thickest film and smallest FWHM.

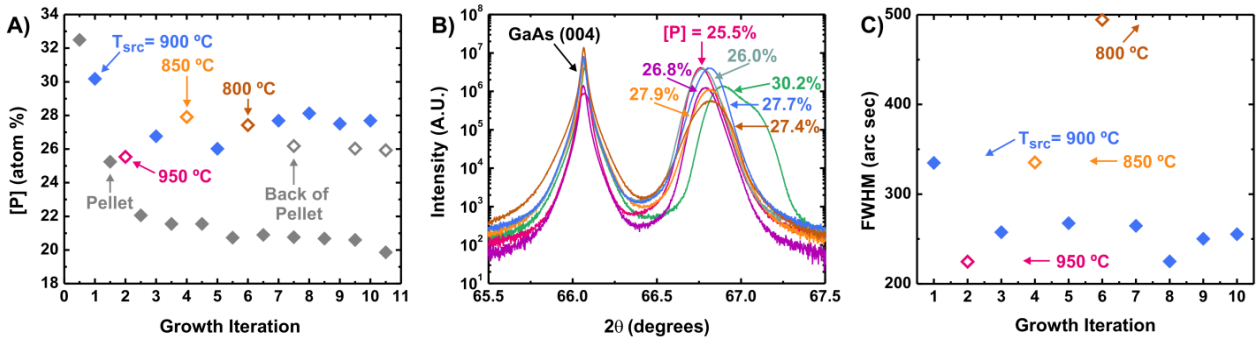

Figure 20: A) Evolution of [P] in the $GaAs_{0.7}P_{0.3}$ source and the resulting varied temperature films. **B)** θ/2θ scans of the first seven varied temperature samples (the others are omitted for clarity). Note the compositional inhomogeneity in sample T1, [P] = 30.2%. **C)** FWHM values from rocking curve scans, which correlate strongly with growth temperature and film thickness. For **A)** and **C)**, films grown at different T_{src} are indicated.

The sintering hypothesis is further supported by the stability of [P] of the source and films over the subsequent growths, although [P] at the source was much lower than that of the films, suggesting depletion at the surface of the pellet. Due to the limited probe depth of XRF, the back of the pellet was measured to confirm that the overall P content remained high. At the end of the growth series, a powder XRD scan of the $GaAs_{0.7}P_{0.3}$ pellet confirmed that the GaAs and GaP powders had formed a solid solution (Figure 21). Because the CSVT transport reactions shown above are each near-equilibrium during growth and growth rates are set by diffusion across the reaction zone,[74] it appears that the film composition follows the average source composition as a result of GaAs and GaP alloying. Thus, the partial pressures of P and As at the source are set by the alloyed source material rather than individual phases.

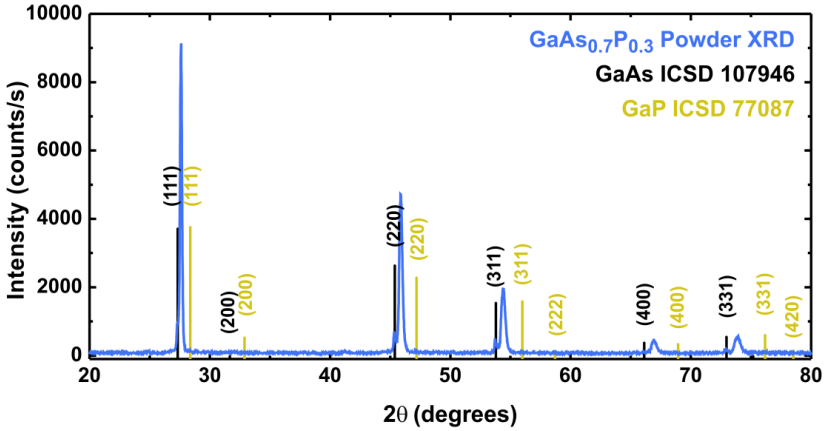

Figure 21: Powder XRD scan showing the analyzed pellet (blue) with the literature peak positions for GaAs and GaP shown (black and yellow, respectively) after ten growths. Minor unincorporated regions exist (based on small GaAs peaks in the powder pattern) but the majority of the pellet has been sintered to a ternary phase.

Electron microscopy (Subtask 3.1)

Although XRD demonstrated that all $GaAs_{1-x}P_x$ films were epitaxial single crystals, they were non-specular. Scanning and transmission electron microscopies were used to elucidate the defects indicated by the large FWHM values for these films. SEM of the composition series showed large, adventitious microstructures, and a large amount of surface texturing which increased with increasing lattice mismatch between the film and substrate (i.e. from [P] = 31% to [P] = 62%, Figure 22A and B). SEM of the temperature series revealed that the adventitious microstructures were a result of the unannealed pellet sources used in the composition series, as the number of microstructures was reduced to near zero over the course of the ten temperature series growths (Figure 22C and D). Finally, a cross-section of the final temperature series sample was prepared using focused ion-beam (FIB) milling. TEM of this sample confirmed the XRD finding that the film was a single crystal and showed a very low incidence of threading dislocations and defects in general (Figure 23).

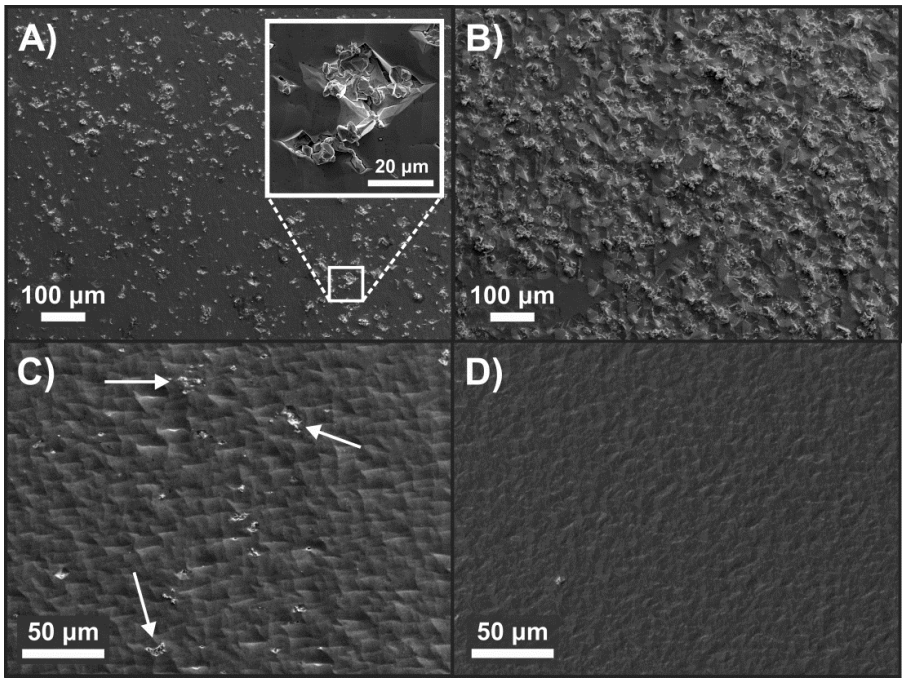

Figure 22: SEMs of **A)** varied composition sample [P] = 31%, inset showing adventitious microstructure. **B)** varied composition sample [P] = 62%, with more microstructures and surface texturing due to mismatch from the substrate. **C)** sample T1 ([P] = 30.2%), showing adventitious microstructures, some of which are indicated by white arrows, and a large degree of surface texturing. **D)** sample T10 ([P] = 27.7%), where microstructures are no longer observed.

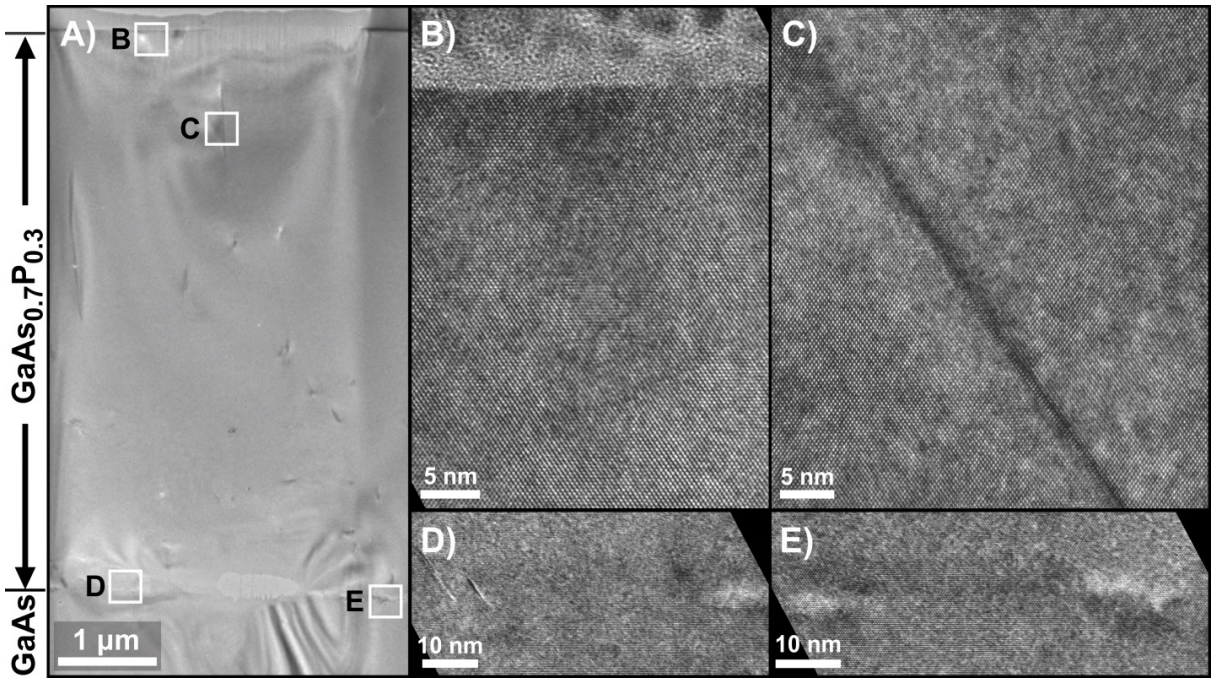

Figure 23: TEM of sample T10 FIB cross-section **A)** Overview of cross-section showing entire thickness of $GaAs_{0.7}P_{0.3}$ film with few defects. The interface with the GaAs substrate is marked. **B)** HR-TEM of the surface showing no defects. **C)** HR-TEM of a dislocation. **D** and **E)** HR-TEM of interface showing no obvious threading dislocations and only few interfacial defects likely related to surface contamination.

Electronic analysis via PEC and Hall effect (Subtask 3.2)

The photoelectrochemical toolbox developed for **Task 1** was utilized here to characterize the $GaAs_{1-x}P_x$ films which had been grown on conductive n^+ substrates (the samples from the variable composition series and the first seven samples of the varied temperature series). This set of non-aqueous PEC techniques allows for the direct measurement of materials properties while avoiding the difficulties associated with forming solid-state junctions on rough surfaces.

Impedance spectroscopy and Mott-Schottky analysis[37,43] were used to measure the dopant densities of the $GaAs_{1-x}P_x$ samples. Although all samples were intended to be undoped, the varied composition sample sources were composed of undoped GaAs and S-doped GaP wafer material, leading to high S incorporation in those films, which was confirmed using time-of-flight mass spectrometry (TOF-SIMS, Table 5). Such efficient S incorporation is expected, given the high vapor pressure of the dopant and previous reports of S-doped CSVT films.[37] For the varied temperature samples, the dopant densities were the same within error (Table 5); TOF-SIMS shows lower [S] in both the GaP source for these samples and the resulting films, suggesting that there may be another contributing dopant which has not been identified.

Table 3: Measured [S] from TOF-SIMS compared to N_D from electrical measurements (all electrochemical impedance except for T9, Hall effect). * indicates that the GaP RSF, rather than GaAs, was used to determine the dopant density.[75]

Series	Sample	Film [P] by XRD (atom %)	[S] by TOF-SIMS (cm^{-3})	N_D (cm^{-3})
Composition GaP Wafer*	--	--	6.2×10^{17}	--
Temperature GaP Wafer*	--	--	4.7×10^{16}	--
Varied Composition	C1	31.4	1.9×10^{18}	$2.1 \pm 0.8 \times 10^{17}$
	C2	36.1	1.2×10^{18}	$2.6 \pm 0.6 \times 10^{17}$
	C4	52.1	3.2×10^{17}	$3.7 \pm 0.3 \times 10^{17}$
Varied Temperature	T1	30.2	3.2×10^{16}	$3 \pm 1 \times 10^{17}$
	T3	26.8	4.3×10^{17}	$3.0 \pm 0.1 \times 10^{17}$
	T5	26.0	2.2×10^{16}	$2.1 \pm 0.2 \times 10^{17}$
	T7	27.7	3.4×10^{16}	$2 \pm 1 \times 10^{17}$
	T9	27.5	2.1×10^{16}	$1.3 \pm 0.3 \times 10^{17}$

Illuminated PEC was also used to probe the *J-E* characteristics of the $GaAs_{1-x}P_x$ samples. For the composition series (Figure 24A), J_{SC} decreased with increasing [P], as increasing [P] increases E_g, decreasing the absorbed wavelengths of light, and for [P] ≥ 44%, the band gap becomes indirect. Increasing E_g also increased V_{OC} for all samples over that of GaAs. For the temperature series (Figure 24B), films grown at T_{src} = 900 °C showed the best overall *J-E* characteristics, as well as good reproducibility. The complete results for both series are tabulated in Table 6.

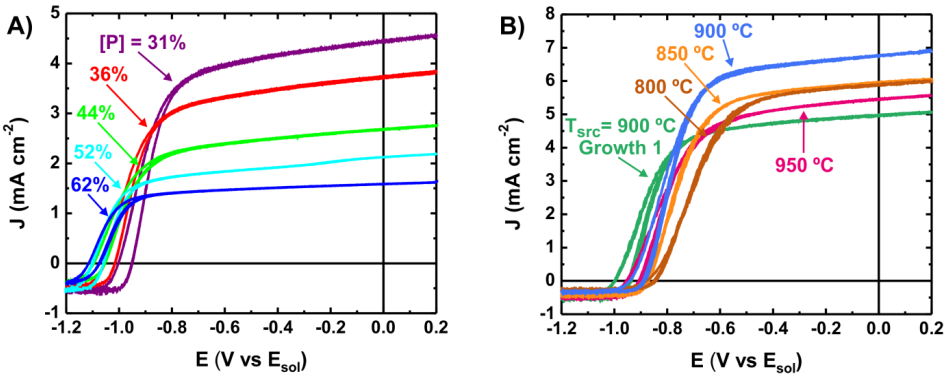

Figure 24: Representative JV curves. **A)** The decrease in J_{SC} across the composition series with increasing [P] is consistent with increasing E_g and the shift from direct to indirect E_g. **B)** The temperature series shows the best *J-E* characteristics for the samples grown at 900 °C; samples T3 and T5 have similar characteristics to T7 and therefore are omitted here. The compositional inhomogeneity of sample T1 (30.2%) appears to have reduced J_{SC}.

Table 4: PEC *J-E* and spectral response measurement results.

	Sample	J_{SC} (mA cm^{-2})	V_{OC} (V vs E_{sol})	L_D (nm)
Variable Composition	C1	4.7 ± 0.2	-0.94 ± 0.03	160 ± 30
	C2	3.9 ± 0.2	-1.02 ± 0.02	140 ± 20
	C3	2.7 ± 0.6	-1.098 ± 0.007	Indirect E_g
	C4	2.1 ± 0.1	-1.09 ± 0.02	Indirect E_g
	C5	1.4 ± 0.3	-1.10 ± 0.02	Indirect E_g
Variable Temperature	T1	5.1 ± 0.4	-0.96 ± 0.02	220 ± 10
	T2	5.3 ± 0.3	-0.941 ± 0.008	141 ± 7
	T3	6.4 ± 0.2	-0.93 ± 0.01	260 ± 10
	T4	6.1 ± 0.5	-0.90 ± 0.01	210 ± 10
	T5	6.1 ± 0.4	-0.96 ± 0.01	220 ± 20
	T6	5.8 ± 0.3	-0.877 ± 0.008	160 ± 20
	T7	6.7 ± 0.3	-0.93 ± 0.01	240 ± 20

Reflectivity and spectral response measurements were used in order to determine internal quantum efficiency Φ_{int} using $\Phi_{ext} = \Phi_{int}[1-R(\lambda)]$. The Gärtner equation was then used to model Φ_{int} and extract L_D, assuming that there is no recombination in the depletion region (width W, see above equation (1))[56] The full range of absorption coefficients, $\alpha(\lambda)$, has not been reported for all compositions of $GaAs_{1-x}P_x$. For the purposes of this work, values of $\alpha(\lambda)$ at the band edge for the direct E_g compositions were estimated based on literature values; full details can be found in the publication related to **Task 3**.[38] The measured Φ_{int} for all compositions as well as the Gärtner fits for the relevant samples can be seen in Figure 26; L_D is given for all samples in the previous table. L_D decreases with increasing [P], as expected due to decreasing hole mobility in the films (a result of increasing N_D) and increasing mismatch between the film and substrate lattices. All samples display low Φ_{int} between 500 and 700 nm, which can be attributed to threading and misfit dislocations in the films resulting from the same mismatch.[76] As with the *J-E* measurements, the temperature series samples with T_{src} = 900 °C have the best properties, with the highest L_D.

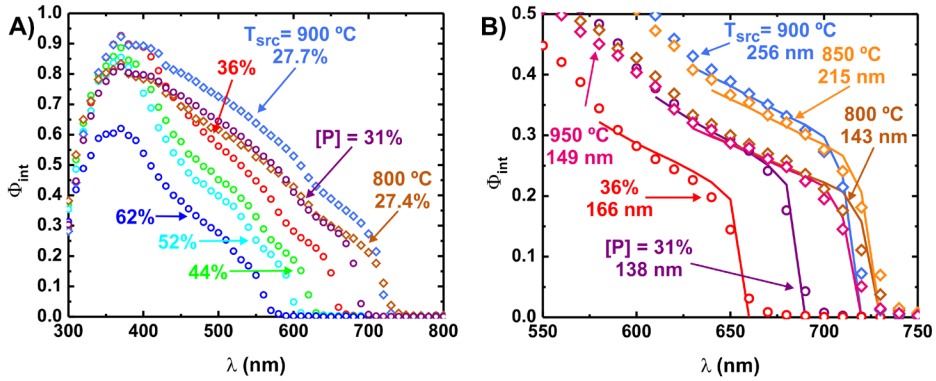

Figure 25: Φ_{int} data for **A)** the varied composition samples and select temperature series samples (T6 and T7) and **B)** at the band edge for representative samples of the temperature series (T2, 4, 6 and 7) and composition series samples C1 and C2. The Gärtner fits to the band edges are shown as solid lines.

Solid-state Hall effect measurements were used to compliment the PEC data. The last three samples of the temperature series were grown on nominally undoped substrates at a single condition, T_{src} = 900 °C. All three films were found to be *n*-type with measured dopant densities in agreement with electrochemical impedance and TOF-SIMS measurements. The Hall electron mobility μ_e was 1200 ± 300 cm^{-2} V^{-1} s^{-1}, in good agreement with the report of Tietjen and Amick.[77]

Milestone (Task 3): $GaAs_{1-x}P_x$ with 0.2 < x < 0.8 deposited by CSVT on GaAs wafers with doping concentrations of 10^{17} to 10^{18} cm^{-3} with PEC response, lifetime, and mobility characterized.

This work demonstrated that $GaAs_{1-x}P_x$ can be grown via CSVT heteroepitaxially on GaAs substrates over a wide range of compositions, 0.25 < *x* < 0.65. Growth temperature, T_{src}, has no major effect on phosphorous transport and incorporation within the range studied. Because all compositions transported with ~10% P loss from source to substrate, it can safely be assumed that the complete range of $GaAs_{1-x}P_x$ can be grown using this method. The desired range of dopant densities, between 10^{17} and 10^{18} cm^{-3}, was obtained using undoped and doped sources. All compositions of $GaAs_{1-x}P_x$ showed reasonable electronic quality measured via PEC *J-E* and spectral response measurements; this quality was confirmed by Hall effect.

Overall, the electronic quality of the $GaAs_{1-x}P_x$ grown via CSVT was promising, but leaves room for improvement. This is especially evident in the decreased J_{SC} for all film compositions, a result of low Φ_{int} and L_D values, compared to MOCVD- or MBE-grown materials which utilize compositional buffers in order to improve film quality.[78] The development of a method for compositional grading by CSVT should help reduce crystalline defects, and therefore improve the electronic quality in future materials. Adventitious microstructures (Figure 22) resulting from particulate transfer from the source may also have contributed to a decreased L_D, impacting J_{SC} and V_{OC}.

These results represent an important step toward the use of CSVT for more-complicated device architectures which employ ternary III-Vs, such as homojunction cells requiring window layers and tandem devices. Further improvements to the growth process, such as elimination of particulate transfer *via* extended pre-growth sintering, and the development of a method to deposit compositionally graded buffer layers would substantially improve the electronic properties of CSVT $GaAs_{1-x}P_x$. This study was

recently published in *Journal of Materials Chemistry A*.[38] Future work related to this task will be focused on developing transport conditions for $GaAs_{1-x}P_x$ deposition using Cl-mediated CSVT, which should also improve materials quality by reducing possible O-incorporation and improving N_D control.

Future work: Development of $In_{0.5}Ga_{0.5}P$

We have also confirmed that it is possible to deposit $In_{1-x}Ga_xP$ films using mixed InP/GaP sources. A pellet was prepared with equal mole concentrations of In and Ga, and several films were grown from this source. As with $GaAs_{1-x}P_x$, a solid solution was formed after a few growths, and the fourth growth from the pellet produced an $In_{1-x}Ga_xP$ film with $x \approx 0.5$ which was nearly latticed-matched to the GaAs substrate (Figure 26). These results are encouraging for the development of CSVT passivating window layers for GaAs devices.

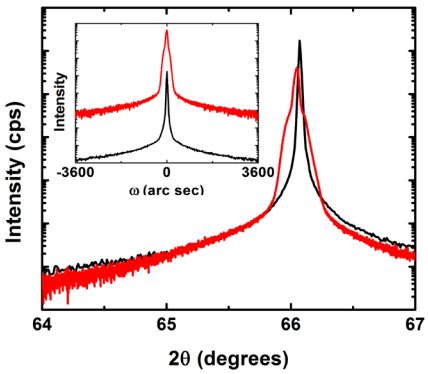

Figure 26: 2θ XRD curve for showing the (004) reflection for an $In_{1-x}Ga_xP$ film (red curve) which is nearly lattice-matched to the GaAs substrate (black curve). Inset: Rocking curves for the film and substrate (004) peaks.

Task 4: Nanopatterning to enable the vapor transport deposition of high-performance III-Vs on Si

GaAs-on-GaAs selective area epitaxy

Crystal growth and structure (Subtask 4.1)

Initial explorations of GaAs-on-GaAs selective area epitaxy were performed via photolithography with a square grid of circular holes of various sizes and spacings in a SiO_x mask. The commercially available GaAs wafer orientations (i.e. (100), (110), (111)A, and (111)B) were coated with electron-beam SiO_x, patterned, and then used as substrates in order to identify the most desirable microstructure morphologies. For initial experiments, the growth time, T_{src}, and ΔT were fixed; commercial (100) GaAs was used as a source. Based on these experiments, the (100) and (111)B wafer orientations were selected for further development.

A second photolithography mask was designed with a hexagonal array of 1 μm holes with 2.5 μm pitch. Initial growths on (111)B orientated wafers indicated that different growth parameters would be necessary in order to grow structures ideal for device applications (height h > 1 μm). Iteration of growth conditions lead to the development of a two-step growth process, where a long, small ΔT step for nucleation is followed by a short, large ΔT step, allowing for additional growth in the <111> direction

(Figure 27A and B). In contrast, optimal growth conditions for microstructure growth on (100) oriented wafers are consistent with GaAs film growth, requiring a moderate ΔT = 20 °C; however, [H_2O] was lowered to 500-1000 ppm in order to slow transport and help prevent structure merging and overgrowth (Figure 27C and D).

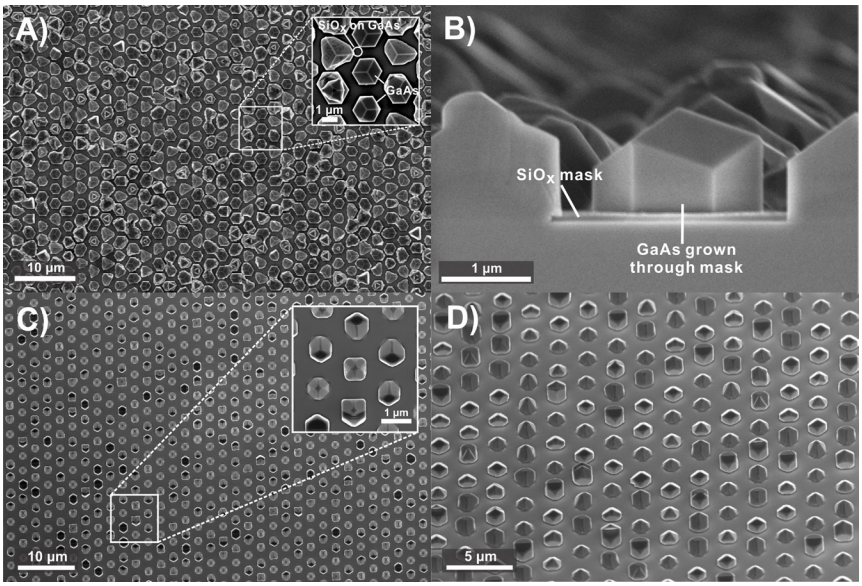

Figure 27: SEMs of microstructure growth. **A)** Plan-view and **B)** cross-section of (111)B microstructures with optimized growth conditions T_{src} = 850 °C, ΔT = 10 °C for 10 min, 50 °C for 90 s **C)** Plan-view and **D)** 45° tilt of (100) microstructures with optimized growth conditions T_{src} = 850 °C, ΔT = 30 °C for 10 min

Optimized SAE on the (111)B and (100) facets provided structures which could be modelled using software such as *Crystal Maker*. The terminating facets are consistent with those identified by Ikejiri, et al. in their study of microstructure SAE in MOCVD for structures grown under high temperature and low As pressures,[79] although the (111)B microstructures terminate with {110} facets rather than a flat {111}B facet, which was also observed in a different report.[80] The terminating facets of these structures represent the slowest-growing crystal directions for these structures.

Characterization by XRD, TEM, and PEC (Subtask 4.2)

High-resolution X-ray diffraction was used as an initial method of quantifying microstructure quality. FWHM values from rocking curve measurements of the bare wafer substrates and optimized microstructure films were compared, using the (111) reflection for the (111)B-oriented samples and (004) reflection for the (100)-oriented samples (Figure 28). Only a small increase in FWHM is observed with microstructure growth in each case, indicating that they are epitaxially oriented to their substrates.

While the computer models can represent the average structures observed in (100) and (111)B growth, there is local variation which cannot easily be modelled. In order to investigate the cause of the structure-to-structure variation (seen in Figure 27), we used FIB milling to produce TEM cross-sections of the microstructures (Figure 29). We observed two important characteristics: very clean interfaces between the GaAs substrates and microstructures, and the presence of twin plane defects in both the

(111)B and (100) samples. These defects occur in the <111> growth direction, when the symmetry across a plane is rotated by 180° relative to the original growth.[81]

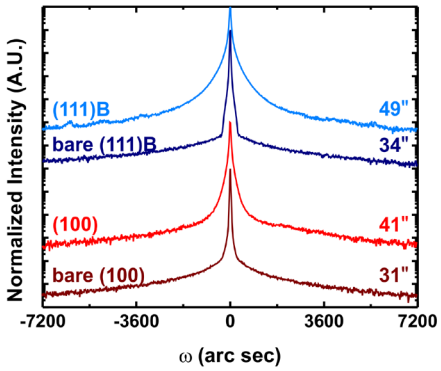

Figure 28: High-resolution rocking curves comparing FWHM of the bare commercial (100) and (111)B substrates to those of the microstructured (100) and (111)B samples.

For the (111)B sample, such defects occur parallel to the growth interface, and are very well-defined, single twins. The low incidence of the twins is remarkable as twinning is well known to occur in zinc blende structures grown by SAE,[82] and can occur frequently, with densities around 10 twins/100 nm height.[80] There also appears to be no correlation between the position of the twins in the microstructures and their external morphology. In contrast, we observe multiple closely-stacked twins in the <111> direction in the (100) microstructures, with positions corresponding to edges of the SiO_x mask vias. These twinned regions do correlate to the observed morphology of the microstructures as they originate at the edges of the SiO_x mask.

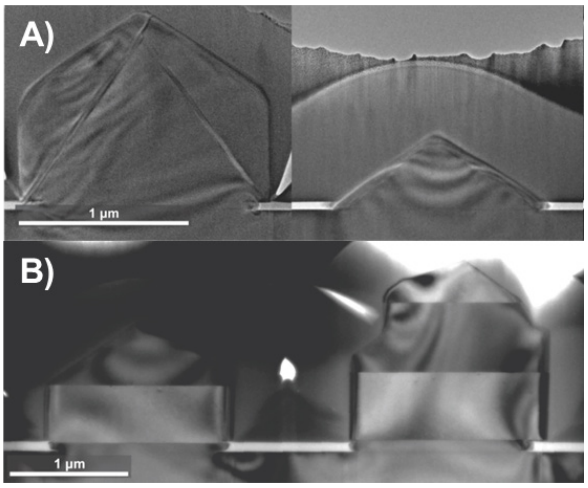

Figure 29: Cross-sectional TEM of **A)** (100) and **B)** (111)B GaAs microstructures. Note the stacks of defects present in the larger (100) microstructure which originate at the edge of the SiO_x mask, and the single twin plane defects parallel to the growth surface in both (111)B microstructures.

Twin plane defects are known to have deleterious effects on the electronic properties of micro- and nanostructures,[82] so we set about quantifying the *J-E* characteristics of the GaAs-on-GaAs SAE samples. The PEC toolbox heavily utilized in **Task 1** and **Task 3** was once again useful here, as it allows for a direct ensemble

measurement of the properties of thousands of microstructures on an electrode, as has been demonstrated with MOCVD-grown GaAs nanowires.[83] We have previously provided proof-of-concept that nanostructured GaAs can provide high J_{SC} using GaAs surfaces that we electrochemically anodized to introduce controlled nanostructure.[84]

Representative illuminated *J-E* curves for both (100) and (111) microstructure orientations are shown in Figure 30. The open-circuit potential V_{OC} of both types of microstructures is slightly smaller than that of a bare GaAs wafer, which is to be partially expected given the dependence of V_{OC} on surface area, but also suggestive of lower electronic quality relative to the CSVT films. The continually increasing current in forward bias observed for both of these samples before removal of their dielectrics is attributable to carrier surface recombination occurring at the unpassivated GaAs surface below the dielectric, as those areas still generate some photocarriers during these experiments.

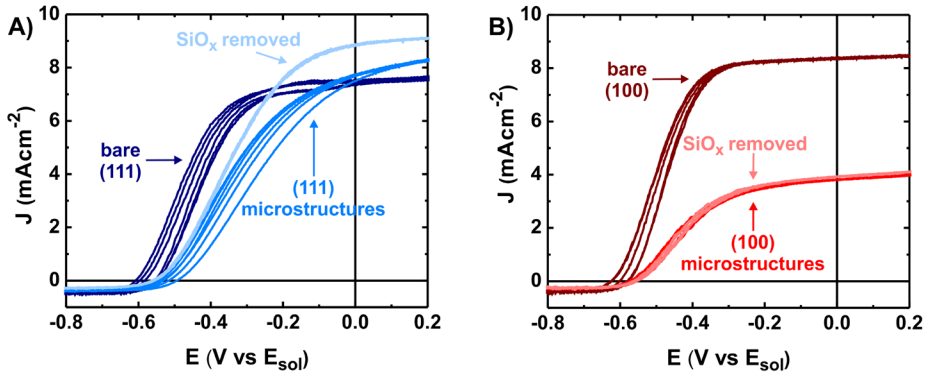

Figure 30: Representative illuminated JV curves for **A)** (111) and **B)** (100) microstructures. The (111) microstructures initially out-perform the bare (111) highly-doped substrate, and their performance is improved with removal of SiO_x. Conversely, the performance of the (100) microstructures is far below the bare (100) highly doped substrate, and does not improve with etching of the dielectric.

Removal of the SiO_x mask using HF slightly improved the photoresponse of the (111) microstructures, as the underlying GaAs substrate contributed some photocurrent. However, the same process had a negligible impact on the (100) microstructures, suggesting that the substrate had become damaged at some point during processing. This was confirmed by conducting the same experiment using a commercial GaAs wafer which had been coated with SiO_x and then run through the microstructure growth process, which also showed no increase in photocurrent after the dielectric mask was removed. The sample was etched back ~ 1 μm without restoring the photocurrent.

We attribute the loss of photocurrent in this case to diffusion of Si from the surface layer into the substrate during growth. Si is known to diffuse faster into (100) GaAs than (111), a likely explanation for the high photocurrent observed for the (111) microstructures and the fact that J_{SC} increased after the SiO_x was removed from those samples. In order to confirm this hypothesis, we used spun-coat Al_2O_3 as an alternative dielectric for another (100) microstructure growth. No major differences were observed in the crystal quality of these microstructures (by SEM or by XRD, with FWHM = 35 arcsec). PEC characterization of these samples is ongoing and suggestive that the Al_2O_3 dielectric preserves the electronic quality of the microstructures and the substrate through the high-temperature growth process.

Further characterization

The investigation of GaAs-on-GaAs SAE microstructures is nearing completion. We plan to continue PEC characterization, determining Φ_{int} using spectral response and sample reflectivity and accounting for the filling fraction of microstructures on the surface. The SiO_x-(100) microstructure samples will be measured in addition to the more promising Al_2O_3-(100) and SiO_x-(111) microstructures in order to help confirm our Si-diffusion hypothesis. We will also use TOF-SIMS of a Te-doped (100) commercial GaAs wafer which was thermally cycled with SiO_x or Al_2O_3 as a capping dielectric layer in order to experimentally confirm the diffusion of Si into the substrate.

$GaAs_{1-x}P_x$-on-GaAs selective area epitaxy (Subtask 4.1)

We have begun to explore the growth of $GaAs_{1-x}P_x$ microstructures by SAE. A $GaAs_{0.7}P_{0.3}$ pellet was used as the source for these experiments, and growth on a patterned SiO_x-(111) substrate was conducted using (111) microstructure growth parameters (described above). SEM and TEM of the resulting microstructures can be seen in Figure 31. By SEM, the morphologies of the (111) $GaAs_{0.7}P_{0.3}$ microstructures are more regular than their GaAs counterparts, likely a result of lower T_{src} and therefore lower growth rate for this sample than the optimal $GaAs_{1-x}P_x$ growth temperature (T_{src} = 900 °C). These microstructures have exposed {111} facets at their tops, confirming a slower growth rate in that direction. Small defects are visible on the structures by SEM, which are further illuminated by cross-sectional TEM. No twin plane defects are evident in the $GaAs_{0.7}P_{0.3}$ microstructure, but an array of threading and misfit dislocations are apparent. These defects originate from the lattice mismatch from the GaAs substrate.

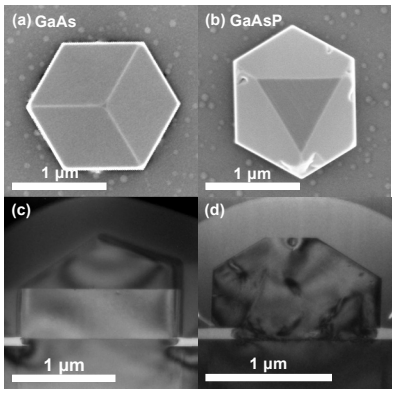

Figure 31: A) GaAs and **B)** GaAsP microstructure on GaAs (111) by selected-area epitaxy. **C)** and **D)** show cross-sectional TEM images prepared by FIB. The GaAs microstructures show twinning defects, while the GaAsP ones show a few interface dislocations due to the 1.3% lattice mismatch, but no twins.

Large-area GaAs growth on Si (Subtask 4.1)

A variety of surface preparations and growth conditions were explored for depositing epitaxial films of GaAs on Si, but only polycrystalline layers could be obtained. We believe that this is due to the irreversible formation of SiO_x due to the use of water vapor as a transport agent. We have proposed that the best strategy for growth on Si using CSVT is to replace the transport agent with a halide such as HCl.

To circumvent Si interface oxidation we elected attempted to introduce a Ge interlayer on top of the Si substrate. Such “virtual Ge” layers have a number of

advantages. Ge has a small lattice mismatch with GaAs, so threading dislocations can be eliminated within the group IV layer, e.g., by cyclic or laser annealing and by patterning small areas of Ge to allow dislocations to terminate at edge sites.[85] The most important advantage in this case is that the oxides of Ge are volatile (in fact, Ge itself can be deposited by H_2O CSVT) and so epitaxial growth is not impeded.

There are a number of previous reports of GaAs grown on Ge by CSVT, in which the source and substrate temperatures range from 700 °C to 900 °C.[86] These films are all reported to be epitaxial, though little detail is given to the growth mode or resulting surface morphology. A more detailed report of the growth mode in CSVT is given by Lalande,[40] who found that smooth growth can be achieved by a temperature inversion step which removes the Ge surface oxides prior to growth. For GaAs grown without this inversion step, anti-phase boundaries are reportedly formed which prevent coalescence of the islands into a single smooth surface (e.g., the streaks visible in the upper portion of Figure 32).

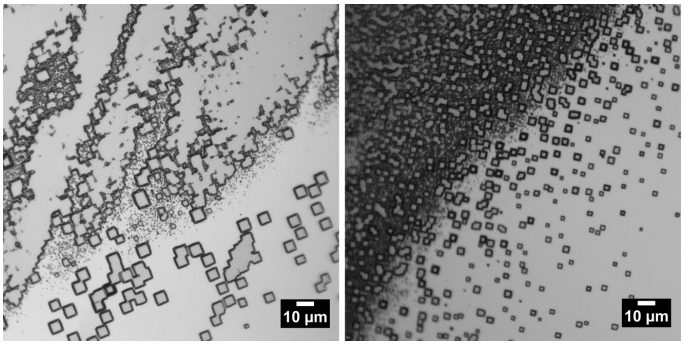

Figure 32. Optical microscope images of GaAs grown on a Ge wafer with a substrate temperature of 760 °C. Bare Ge and isolated GaAs islands are visible in the lower right corner, where the film is covered by the quartz spacer during growth. Left: source temperature 800 °C. Right: source temperature 820 °C.

With a temperature inversion step, we found that regular pyramidal structures can be formed on 5 µm sized square virtual-Ge mesas (Figure 34). These appear to have the same faceting as GaAs microstructures grown on (100) GaAs substrates, but without truncated corners since the mesas in the case are square rather than circular.

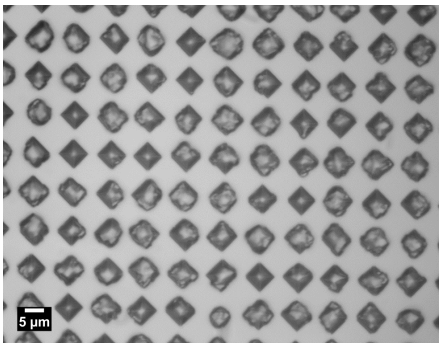

Figure 33: GaAs microstructures grown on Ge mesas, on a Si wafer. The Ge mesas were etched from ~50 nm films deposited by thermal evaporation on a (100) Si wafer, and subsequently treated by a cyclic thermal annealing process.

Summary of Major Accomplishments

We have demonstrated major progress in the science and photovoltaic device implementation of CSVT-based III-V materials. Our primary accomplishments include:

- Demonstrated that the electronic quality of CSVT material can be excellent, with mobilities approaching those obtained by MOCVD and that control over doping is possible using mixed powder solid sources. (Achieved Milestone ST 1.1) This is an essential “first-step” in using CSVT for PV applications.
- Demonstrated excellent minority carrier collection (near unity) in test photoelectrodes fabricated from CSVT GaAs, consistent with the high (majority carrier) electronic quality measured by Hall Effect. (Achieved Milestone ST 1.3) This was the first measurement of minority carrier collection properties of CSVT devices and the long diffusion lengths found (> 5 μm) were again consistent with excellent electronic properties of the absorber film.
- Fabricated the first *pn* junction photovoltaics by CSVT with open circuit voltages reaching 915 mV and internal quantum efficiency > 0.9 without surface passivation. (We thus *nearly* achieved Go/NoGo-1, which had the aggressive goal of V_{oc} > 950 mV and internal quantum efficiency > 0.9). Such CSVT pn junction PVs had never before been made so this work is an important proof of principle for the technology. We also found that morphological defects are the main source of film performance heterogeneity.
- Deposited $GaAs_{1-x}P_x$ from mixed powder sources with compositions and band gaps (~1.7 eV) suitable for top-cells on Si (Achieved Milestone T-3). While $GaAs_{1-x}P_x$ had been grown previously by CSVT we were the first to report comprehensive structural and electronic characterization. Our TEM imaging shows defects which are likely related to lattice mismatch and that can be eliminated by strain relief strategies.
- Showed selective-area epitaxy using CSVT, an essential step in implementing a nano- or microstructure based interface strain-relief layer for III-V on Si devices. While there had been previous reports of selective area epitaxy at the 10-100 micron scale, we uncovered the growth modes at the 1-2 micron scale which is approaching the scale relevant for interface misfit dislocation relief in heteroepitaxial growth on lattice-mismatched substrates.
- Transferred knowledge on photoelectrochemical semiconductor materials characterization to the Molecular Foundry, a DOE user facility. (Achieved Final Deliverable 2).

We filed a full patent application on the powder-precursor vapor transport deposition process and its application to III-V PV technology (US20150303347). We presented the work at National MRS and PVSC meetings and at key national laboratories, such as NREL and LBNL, and the results have all been published (or will shortly be submitted for publication).

Publications

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9) Boucher, J. W.; Greenaway, A. L.; Egelhofer, K. E.; Torrigino, B. B.; Aloni, S.; Boettcher, S. W. Impact of Surface Morphology on GaAs Homojunction Solar Cells Grown by Close-Spaced Vapor Transport. *In Prep.* **2016**.

Challenges Identified

We have also identified challenges with the current CSVT process. We discuss our strategies for directly addressing each of these in the following “path forward” section.

- The use of H_2O limits the ability to deposit films from precursors, or onto substrates, that are irreversibly oxidized under our growth conditions. This has precluded the growth of Al-containing alloys and has prevented heteroepitaxy on Si. For this

reason, we were unable to complete the final project milestone (ST 4.2) and deliverable (FD-1).

- We have found issues with reproducibility of the process and film morphology during growth that we believe are related to particulate contamination of the substrate in the simple generation-one reactor design. Residual gallium oxides may also be contributing to surface defects discussed above, as has been found in MBE.[63–65]

Path Forward and Potential Manufacturing Challenges/Approaches

The primary challenges we faced in this project were associated with limitations in the deposition hardware. Our first priority moving forward is thus to design, build, and qualify improved deposition hardware. To do this we have partnered with Robert Weiss at Malachite Technologies, a small company specializing in deposition equipment. Weiss is an expert in custom physical vapor deposition technologies (e.g. sputtering from his time as CTO at Intevac and DayStar) and has a long interest in low-cost III-V technology.

Our envisioned Gen-II reactor uses HCl as the transport gas and has dedicated growth stations for each layer in the cell stack (Figure 34). "Cl-CSVT" resolves the problems found with Al and Si while allowing lower growth temperatures. The dedicated growth stations should allow better interfaces, faster experimentation, and more sophisticated device structures. HCl has long been used as a transport agent for GaAs growth and there is substantial evidence from HVPE literature (using Cl to transport group III elements) that it will provide high materials quality and work well for the ternary compositions needed for high-efficiency device architectures.

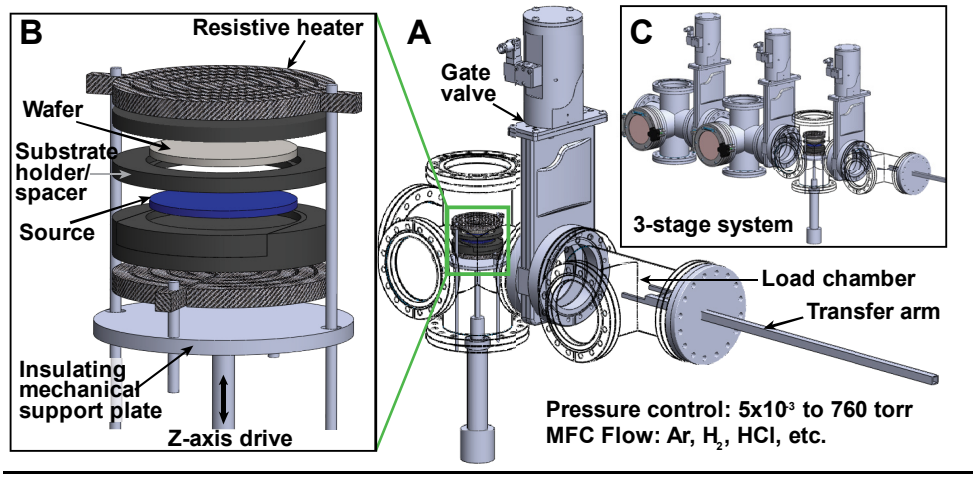

Figure 34: (a) Preliminary design of load-locked Cl-CSVT for high-rate III-V epitaxy. A gas manifold and downstream throttle valve and pump assembly controls pressure and gas composition/flow. (b) Heater assembly in deposition chamber. The wafer sits above the source and is transferred in/out and between stages by a forked transfer arm. (c) Three-stage system for passivated *pn* device development. Component design and testing for this system has already begun and we are working to secure funding.

The Gen-II system should allow us to fabricate, with a much higher degree of reproducibility, passivated GaAs homojunction devices with performance characteristics competitive with MOCVD devices (at least 20% efficiency). It will also allow us to explore a number of new options for growth on Si. For example, we aim to implement a low-cost version of a GaAsP graded buffer layer as well as perform direct GaP-on-Si heteroepitaxial growth. Such structures have been grown by MOCVD and MBE.

These advances will help build the foundation for our ultimate vision for the CSVT technology as a low-cost approach to integrating high-performance III-V semiconductors with inexpensive Si bottom cells in a tandem configuration, such as shown in Figure 35. Prof. Boettcher has, last year, started a collaboration with Prof. Zach Holman (Arizona State University) seed-funded by a Research Corporation Scialog Solar Collaborative Innovation Award ($100k) to augment our studies of III-V's on Si. Holman is an expert in high-efficiency heterojunction Si solar cells and will be a resource and further academic collaborator as the project progresses.

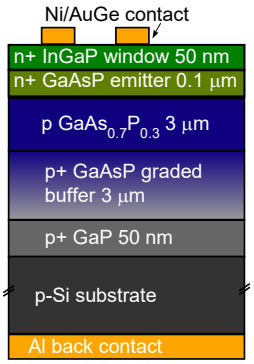

Figure 35: Target CSVT GaAsP on Si device.

We have also started to explore funding opportunities for the next project stage. The technology is currently not at a sufficient technology readiness level for significant commercialization funding. Therefore, we have applied for DOE EERE funding to demonstrate the above proposed advances in materials and device quality, reproducibility, and Si substrate compatibility. If we are successful in this phase of the technology development we believe the timing will be appropriate to solicit (1) innovative companies commercializing III-V PV (e.g. Microlink, Alta Devices) who have indicated interest in low-cost deposition approaches that are compatible with epitaxial layer lift-off technologies,[87] and (2) Si manufacturers (e.g. Solarworld) who will need new strategies to increase efficiencies and continue cost reductions.

Large-scale manufacturing would present a number of additional challenges that have not been explored in this project. High precursor utilization requires a source be used for many growth cycles beyond what is typically performed in a research setting. Even with improved gas confinement, some arsenic may be lost during grow cycles, requiring reprocessing of the source material. Excessive need to reprocess the source could affect ultimate manufacturing feasibility. Manufacturing will also require developing substrate handling technology that will limit contamination between different sources (i.e. composition and doping types) and allow for rapid sample transfer between sources without complete source cooling (which would considerably slow the process).

Ultimately our team sees itself as innovators in deposition rather than engineered systems, and will concentrate our efforts on refinement and early stage demonstration of solid-source III-V deposition. We do not aim to start an independent solar manufacturing company or a new equipment manufacturing company. We plan to engage as early as possible with established companies to promote the possibility of licensing or acquiring our equipment IP, as we have already done with our first patent application (above).

Budget and Schedule:

The table below shows the project spend plan on a per-quarter basis. The planned and actual spending were very similar.

Calendar Quarter	Year	From	To	A. Federal Share Initial Plan totals $450000	B. Federal Share Updated Actuals & Plan	Cumulative Federal Share	C. Recipient Share Initial Plan totals $45000	D. Recipient Share Updated Actuals & Plan	Cumulative Recipient Share
Q4	2012	10/1/2012	12/31/2012	$40,937.00	$155.30	$155.30	$0.00	$0.00	$0.00
Q1	2013	1/1/2013	3/31/2013	$40,937.00	$37,850.03	$38,005.33	$0.00	$0.00	$0.00
Q2	2013	4/1/2013	6/30/2013	$40,937.00	$22,039.30	$60,044.63	$1,744.00	$4,580.28	$4,580.28
Q3	2013	7/1/2013	9/30/2013	$40,937.00	$27,655.63	$87,700.26	$17,170.00	$13,612.23	$18,192.51
Q4	2013	10/1/2013	12/31/2013	$40,937.00	$88,497.95	$176,198.21	$1,744.00	$6,092.57	$24,285.08
Q1	2014	1/1/2014	3/31/2014	$40,937.00	$50,619.04	$226,817.25	$1,744.00	$4,554.35	$28,839.43
Q2	2014	4/1/2014	6/30/2014	$30,000.00	$62,345.49	$289,162.74	$0.00	$1,023.05	$29,862.48
Q3	2014	7/1/2014	9/30/2014	$30,000.00	$22,335.71	$311,498.45	$13,000.00	$13,072.99	$42,935.47
Q4	2014	10/1/2014	12/31/2014	$30,000.00	$48,420.96	$359,919.41	$0.00	$259.98	$43,195.45
Q1	2015	1/1/2015	3/31/2015	$30,000.00	$26,629.68	$386,549.09	$0.00	$25.00	$43,220.45
Q2	2015	4/1/2015	6/30/2015	$30,000.00	$31,966.56	$418,515.65	$0.00	$72.75	$43,293.20
Q3	2015	7/1/2015	9/30/2015	$30,000.00	$21,546.42	$440,062.07	$9,598.00	$0.00	$43,293.20
Q4	2015	10/1/2015	12/31/2015	$24,378.00	$9,937.93	$450,000.00	$0.00	$1,706.80	$45,000.00
Totals				**$450,000.00**	**$450,000.00**	$450,000.00	**$45,000.00**	**$45,000.00**	$45,000.00

The next table shows the spending category breakdown for expenses budgeted versus actual. Most expenditures are similar to those budgeted, with the exception of supplies. As reported to DOE in earlier quarterly reports, the differences are due to changes in the personnel costs. Andy Ritenour won an internal UO Dixon Fellowship which supported a portion of his tuition and stipend. Ann Greenaway joined the project fully supported by an NSF Graduate Research Fellowship. The U. Oregon also lowered the graduate tuition charged to grants by ~$10k/yr. Jason Boucher was supported full-time on the project. Therefore, we were able to use a portion of the budgeted personnel costs to support research through increased supply budget and use of analytical tools.

Object Class Categories Per SF 424a	Approved Budget ($)	Project Expenditures ($)	
		This Reporting Period	Cumulative
a. Personnel	$134,420	$2,927	$119,985
b. Fringe Benefits	$43,217	$932	$32,863
c. Travel	$16,495	$348	$10,323
d. Equipment	$30,000	$0	$33,752
e. Supplies	$10,500	$1,530	$54,045
f. Contractual	$105,000	$4,235	$104,777
g. Construction	$0	$0	$0
h. Other	$72,284	-$265	$49,847
i. Total Direct Charges (sum of a to h)	$411,916	$9,708	$405,593
j. Indirect Charges	$83,084	$1,937	$89,185
k. Totals (sum of i and j)	**$495,000**	**$11,645**	**$494,777**
DOE Share	**$450,000**	**$9,938**	**$450,000**
Cost Share	$45,000	$1,707	$45,000
Calculated Cost Share Percentage	9.1%	14.7%	9.1%

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