U.S. DEPARTMENT OF ENERGY

OAK RIDGE NATIONAL LABORATORY
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High Temperature, High Voltage Fully Integrated Gate Driver Circuit

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Project ID:
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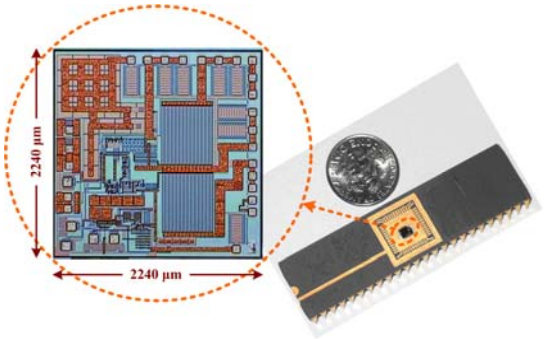
Overview

Timeline

- Start Date: Oct. 2008
- End Date: Sept. 2011
- 20% Complete

Budget

- DOE Share – 100%
- FY09 received: $367K
- FY10 requested: $364K



Barriers

- Highly integrated gate drive
  - Reduced volume and weight
  - Higher temperature tolerance / reduced cooling needs
  - Universal integrated module
- Vehicle Technology Program Targets
  - DOE 2015 target: 105°C coolant

Partners

- Development:
  The University of Tennessee
- Field Testing: GM ATV, AFRL

Objective

- Develop a highly reliable, integrated gate drive circuit that is capable of operating at high temperatures while driving GaN or SiC JFETs or MOSFETs
- FY09
  - Design, fabricate, test a silicon on insulator (SOI) chip that has robustness for wide temperature range (-40°C to 175°C ambient)
  - Incorporate several protective features (over current, over temperature, under voltage)

Milestone

- **August 2009: Successfully demonstrate that the fabricated SOI gate drive chip can act as a gate driver over a wide temperature range for prototype SiC MOSFETs and JFETs obtained from suppliers.**
- *Go/No Go - Ability of SOI chip to drive SiC FET over wide temperature range (-40℃ to 175℃)*

Approach

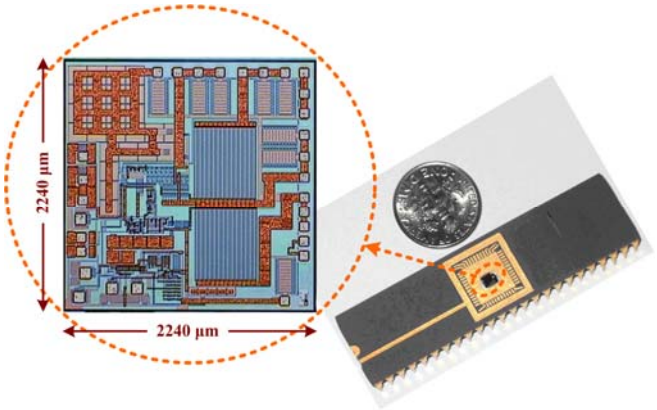
- **SOI-based high-temperature, high-voltage gate driver will be developed that can work up to 175°C ambient.**
- **Improve circuit topology for reliable and repeatable performance at elevated temperatures.**
- **Test prototypes to support a variety of SiC-based or GaN-based power switches (JFETs and MOSFETs) as they become available. Driver designed as a "universal gate drive" to meet various FET specs.**
- **Incorporate protection features, such as short circuit protection, under voltage protection, and embedded temperature sensors to enhance robustness.**
- **Successful execution of this research combined with commercially available WBG-based power switches will help realize high-temperature DC-DC converters and traction drive systems (inverters) for HEVs.**

Description of Silicon-on-Insulator (SOI) Technology

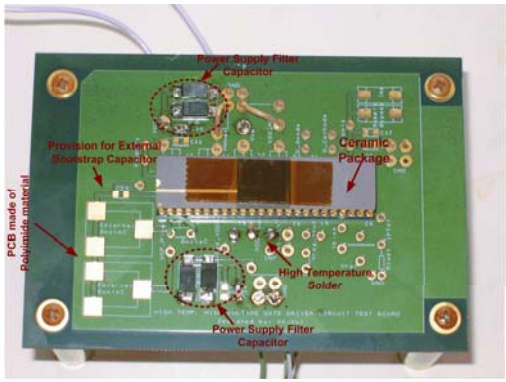
- High-temperature, high-voltage fully integrated gate driver based on Bipolar-CMOS-DMOS on Silicon-on-Insulator (BCD on SOI) technology
- SOI offers inherently low leakage current and latch-up immunity, thus enabling circuits to operate at higher temperature than their bulk Si-based counterparts.
- Novel circuit design approach to provide gate driver circuit performance insensitive to temperature variation

FY08 Technical Accomplishments

(high temp gate drive work funded by a previous project)



Chip size 5 mm^2 (2,240 µm × 2,240 µm)

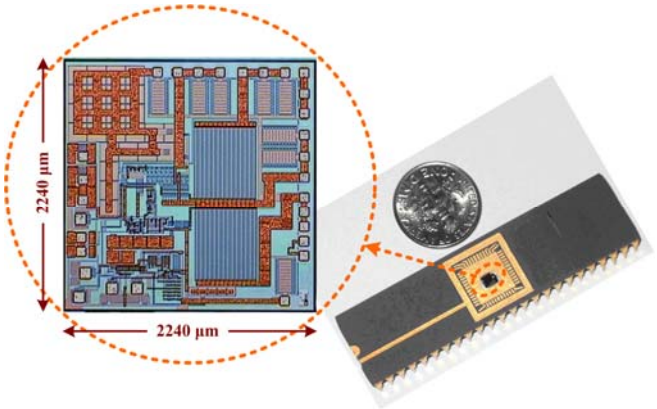


High-temperature polyimide test board

- **Prototype of a high-temperature, high-voltage integrated circuit gate driver, designed and fabricated using a BCD-on-SOI process from Atmel in 2008.**
- **Successfully tested at low voltages (up to 320 V) with SiC MOSFETs and JFETs at 200°C without any heat sink and cooling mechanism.**

Prominent Features of SOI Chip

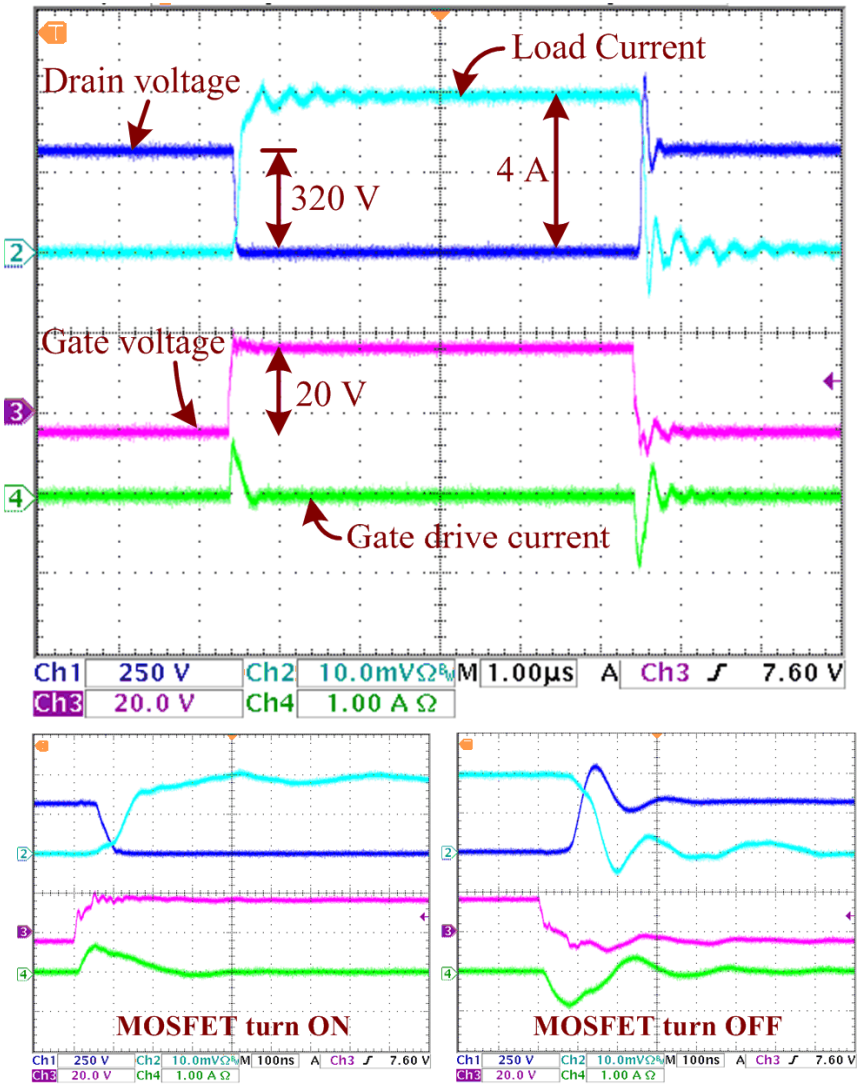
- High source and sink current capability: peak 2.3 A @ 27°C and 1.7 A @ 200°C ambient
- Gate drive supply range from 10 V to 40 V p-p
- High operating temperature: 200°C ambient without any cooling mechanism
- High capacitive load drive capability: 10 nF in < 100ns @ 200°C



Chip size 5 mm^2 (2,240 µm × 2,240 µm)

- Die area of **5 mm^2 (2,240 µm × 2,240 µm)** including bootstrap capacitor, voltage regulator, pad frame, and ESD protections.
- 0.8-micron, 2-poly and 3-metal BCD on SOI process from Atmel has been used.

Driving SiC MOSFET

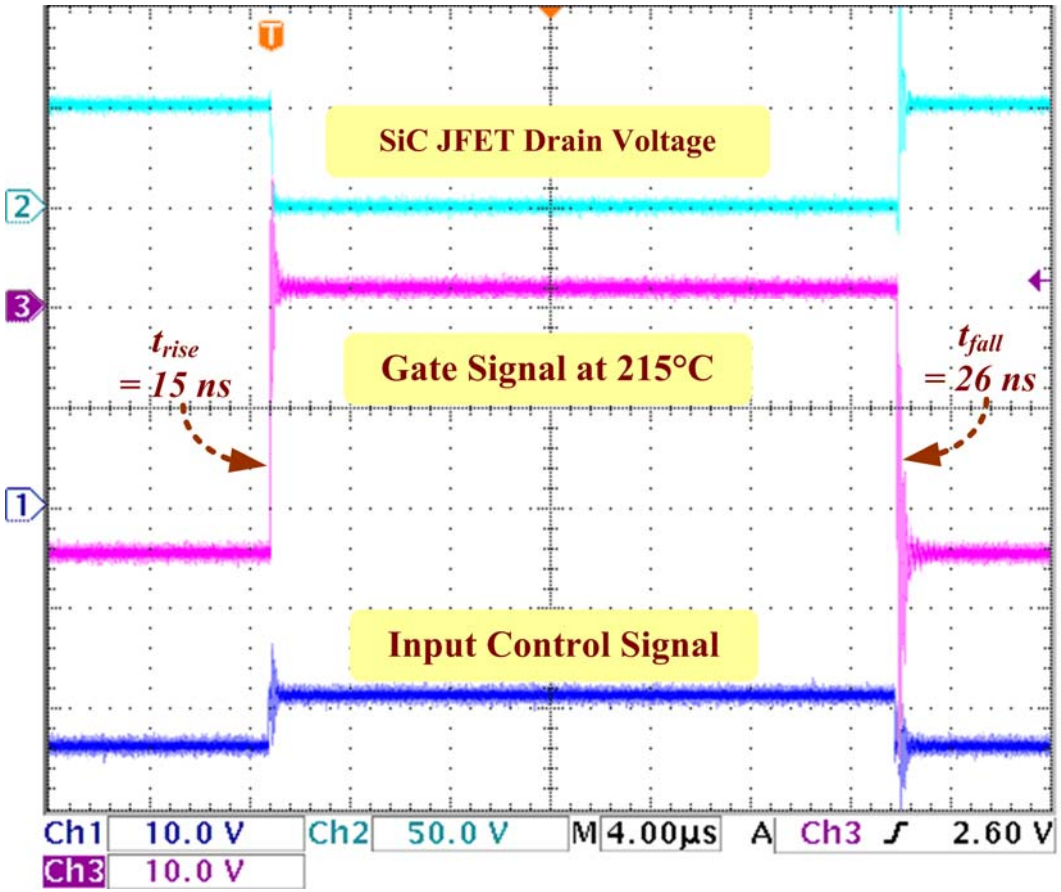


Driving Cree SiC MOSFET with the Gate Driver Chip at 200°C ambient

Rise- and fall-times at different ambient temperatures

Ambient Temp. (°C)	Drain Voltage (V_{DS})		Gate Voltage (V_{GS})	
	t_{rise}(ns)	t_{fall}(ns)	t_{rise}(ns)	t_{fall}(ns)
25	24.1	40.9	42.3	55.6
125	24.8	41.2	43.5	61.1
150	23.5	39.2	43.9	63.7
175	25.2	41.9	43.7	65.5
200	25.1	41.5	43.5	63.3

Driving SiC JFET

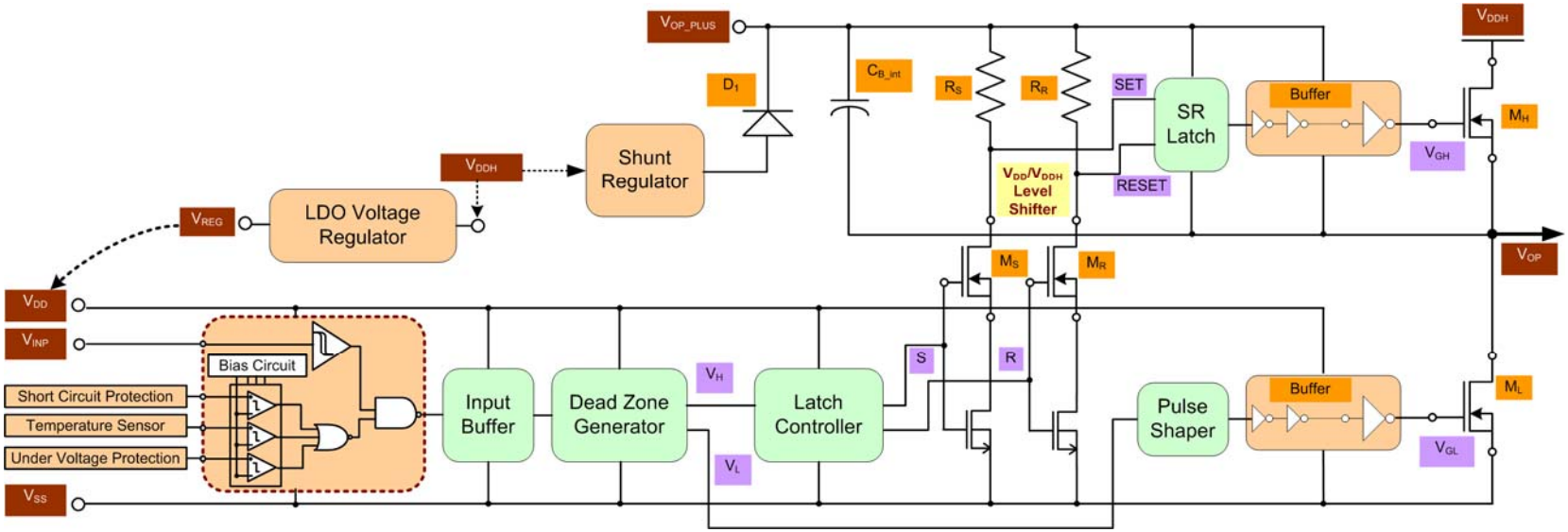


Driving SemiSouth SiC JFET with gate driver chip at 215°C ambient

- SiC JFET used for this test is a normally ON (depletion mode) type device
- Gate voltage applied to the gate of the JFET was +3V to −22V (w/ grounded source)

FY09 Technical Accomplishments

- A new SOI chip has been designed, had layout, post layout simulation and submitted for fabrication in April.
- Redesigned top-side buffer in core gate drive circuit using 5 V PMOS with "neighboring box" and regular 5 V NMOS instead of 45 V devices (PMOS and NMOS). 82% die area savings achieved compared to the previous top-side buffer.
- Additional protection circuitry to turn device off in event of load short circuit, over temperature, and under voltage.



Schematic of prototype SOI gate driver circuit

Future Work – FY09

- Receive fabricated and packaged SOI chips – expected late June 2009
- Fabricate and populate polymide high temperature test board
- Test prototype circuits with SiC power MOSFETs and JFETs

Future Work – FY10 and beyond

- Increase output current rating of gate drive to handle large power electronic modules
- Incorporate digital slew rate control in gate drive so that it can adapt to different devices and not cause transient over voltages during switching by controlling dv/dt during switching.
- Investigate integrating gate drive with SiC switches into an intelligent power module.

Summary

- **A highly integrated, high temperature gate drive is being developed for use with future wide band gap (silicon carbide and gallium nitride) switching devices.**
- **Universal drive that is capable of driving a wide variety of devices including MOSFETs, JFETs, and IGBTs.**
- **Gate drive will be an enabling technology for using power electronics at higher temperatures.**