WBG Gate Drivers for Power Modules

Leon M. Tolbert

Oak Ridge National Laboratory

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Overview

Timeline

- Start – FY13
- Finish – FY15
- 22% complete

Budget

- Total project funding: $700K
  - DOE share – 83%
- Funding for FY13: $600K
- II-VI Foundation: $100K

Barriers

- Converter volume, weight, cost
- Converter high temperature capabilities

Inverter targets

- Power density: 14 kW/l (2020 target)
- Specific power: 14 kW/kg (2020 target)
- Cost: $5/kW (2015 target)

Partners

- **ORNL team members:** Zhenxian Liang, Puqi Ning, Fred Wang, Andy Wereszczak
- **The University of Tennessee:** Ben Blalock, Jeremy Holleman, Kamrul Islam

Project Objective

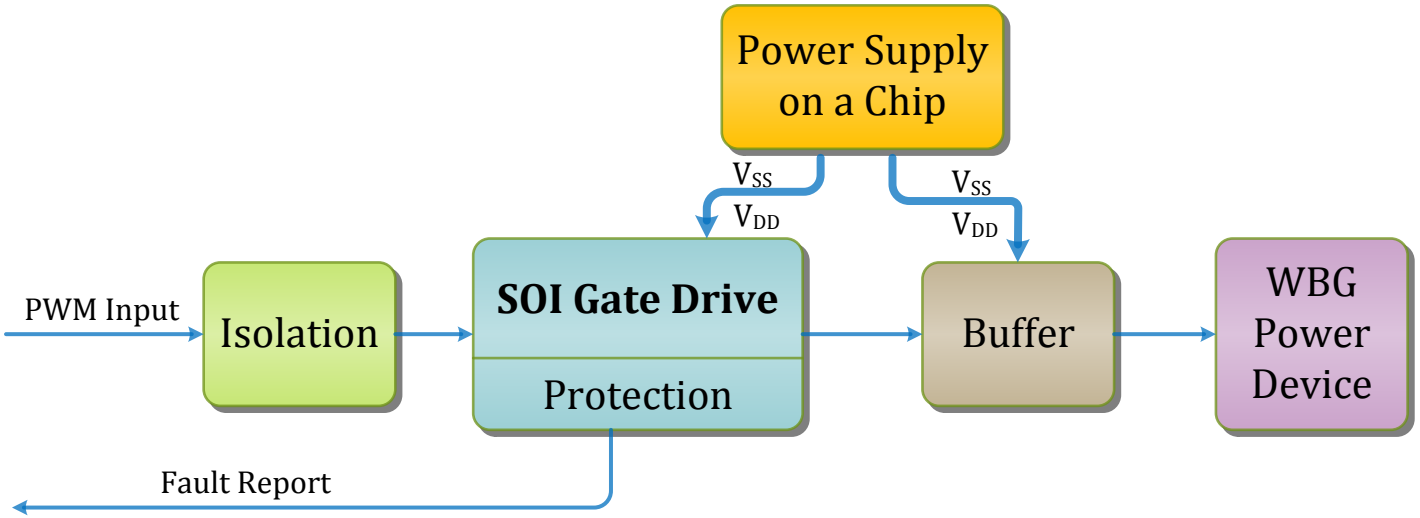
- **Overall Objective**
  - Develop a highly integrated power module phase leg (rated at 1200 V and 200 A) incorporating wide bandgap devices that includes: (1) an integrated gate drive, (2) isolation chip, and (3) power supply, in a package that allows it to work at high temperatures (up to 150°C ambient) and device junction temperatures at up to 200°C.
  - Smart gate drive has protection features, high current capability, and active gate control to minimize switching loss and chance of noise-induced gate turn-on that can lead to shoot-through.
  - Final goal is to produce 55 kW inverter phase leg modules that can work at high temperatures and meet 2020 Targets of 14 kW/l, 14 kW/kg, and 2015 Targets of $ 5 /kW, and 98 % efficiency.
- **FY13 Objective**
  - Design and fabricate high temperature integrated circuits and develop packaging techniques for these and SiC MOSFETs and diodes to build an initial module incorporating gate drive, isolation, and protection.

Milestones

Date	Milestones and Go/No-Go Decisions	Status
Sept 2013	Milestone: Package a SOI gate drive with SiC MOSFET die into a high temperature package.	On schedule
Aug 2013	Go/No-Go decision: Check voltage blocking capability of isolation chip. If insufficient, CHANGE concept.	On schedule

Approach/Strategy

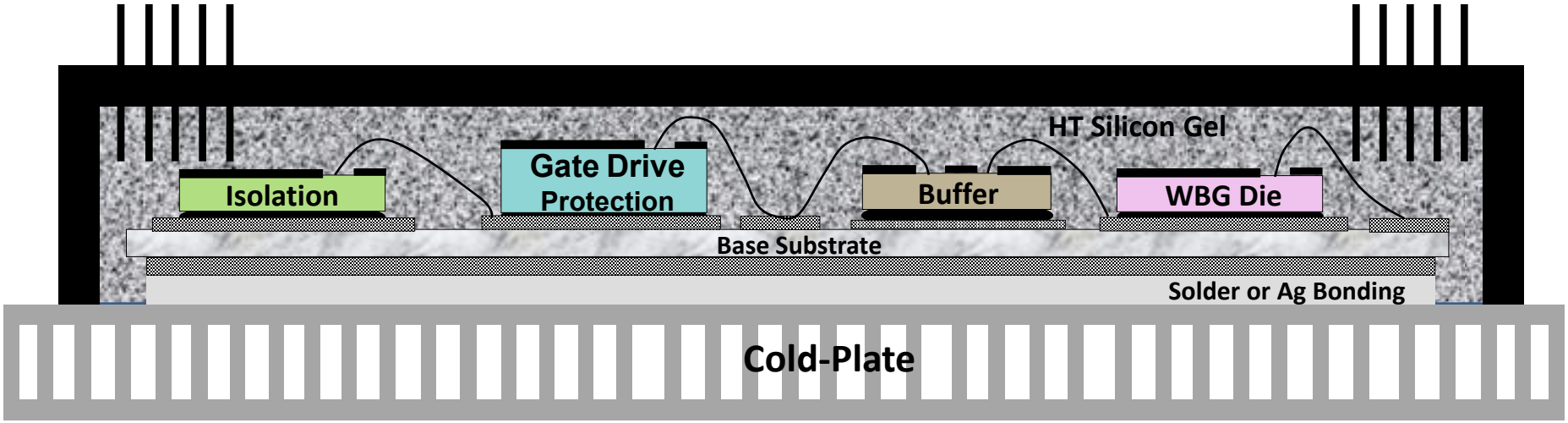
Highly Integrated Power Module



- A new SOI gate drive that improves upon a previous design will be designed and fabricated.
- An isolation chip that can provide galvanic isolation for the gate drive will be designed and fabricated.
- Develop a power supply on a chip that can be used in automotive environments and specifically in a WBG power module.

Approach/Strategy - Packaging Technologies

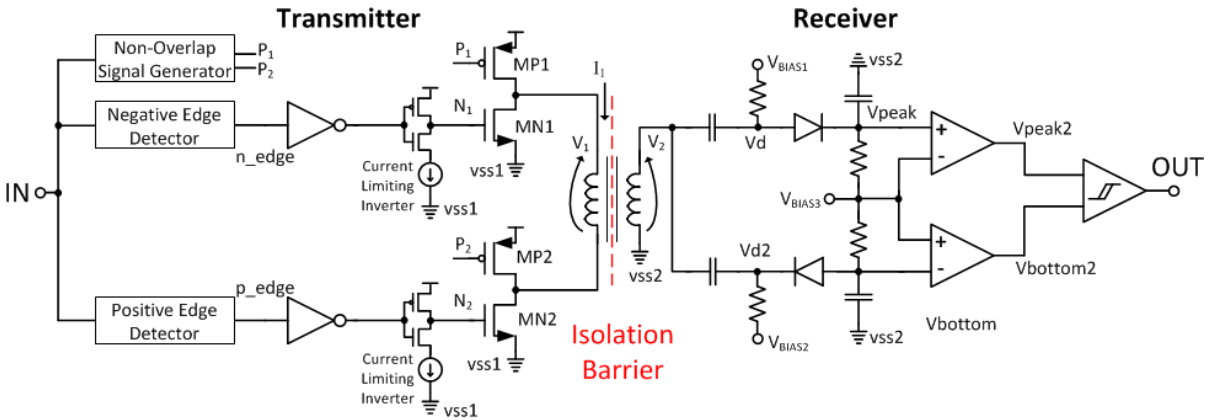
Packaging Structure Schematic
Integrated High Temperature Power Module



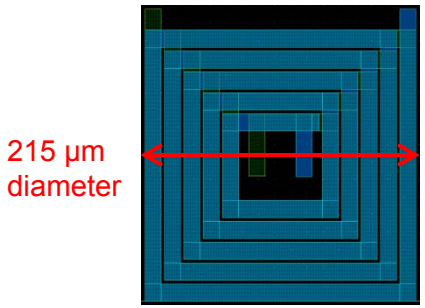
- Packaging focuses on what materials and processes are needed to integrate all of the associated chips and power devices into a module that can function at temperatures greater than 200°C.

Approach/Strategy - Isolation

- Galvanic input isolation is focused on an on-chip transformer isolation design
- Isolation achieved by stacked transformer constructed with metal interconnect
  - Oxide thickness between metal layers limits DC isolation (700 V/μm)
  - Overlap capacitance of coils limits transient noise immunity
- Two chip solution (transmitter and receiver) with on-chip transformer using 5-V CMOS technologies
  - Design will be fabricated in two chip technologies
  - High frequency signal transmission allows smaller transformer area
  - PWM input signal frequency up to 1 MHz

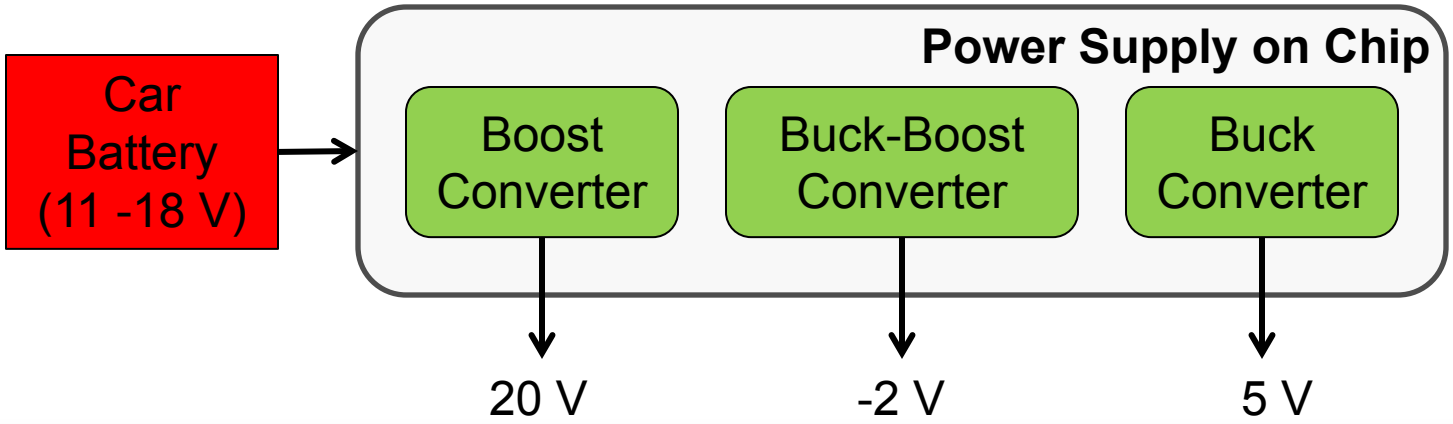


Transformer Layout Example

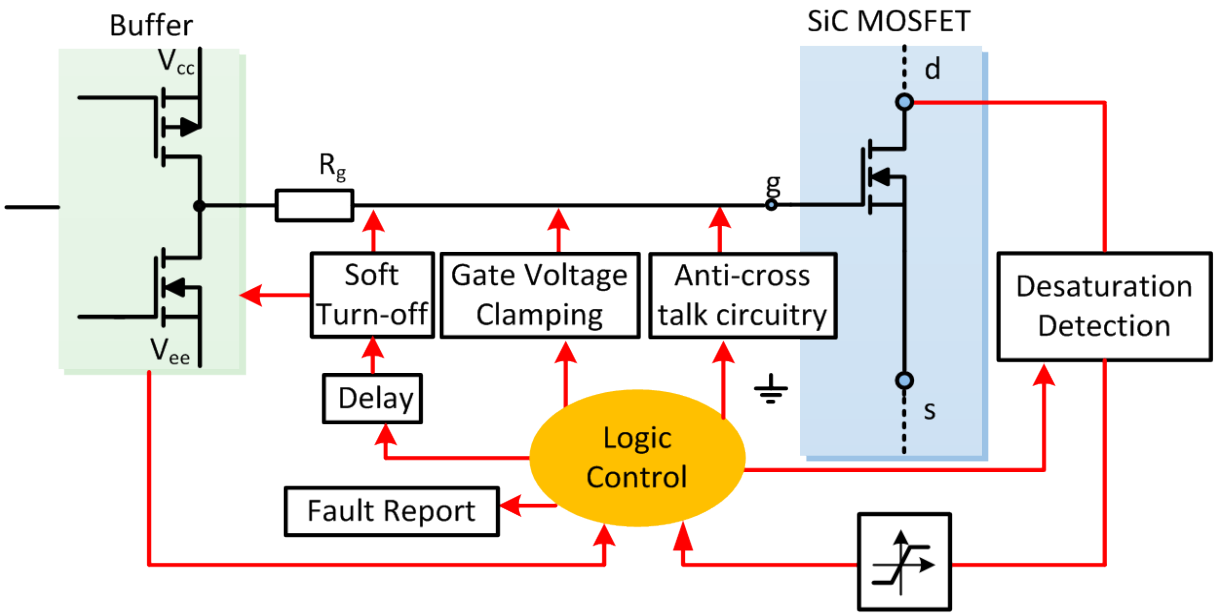


Approach/Strategy - Power Supply on a Chip

- Develop a fully integrated power supply on chip, operational at temperatures greater than 200 °C
  - Power supply will provide a +20 V VDD rail, a -2 V VSS rail, and a +5 V supply
- Each voltage supply will be able to deliver 150 mA and have < 5% ripple
- PWM scheme will be used to regulate the voltage supplies for inputs ranging from 11 V to 18 V



Approach/Strategy – Protection

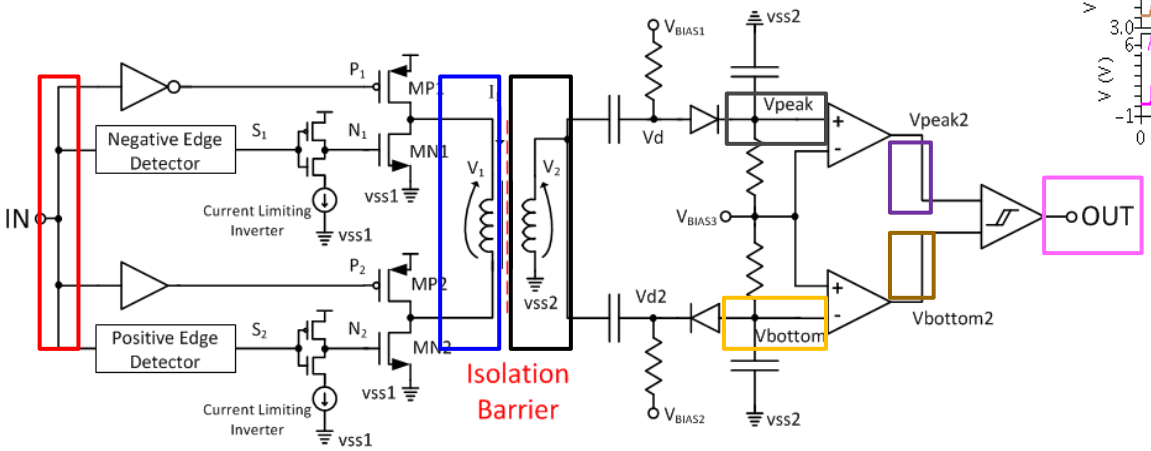


Proposed protection scheme for SiC MOSFETs

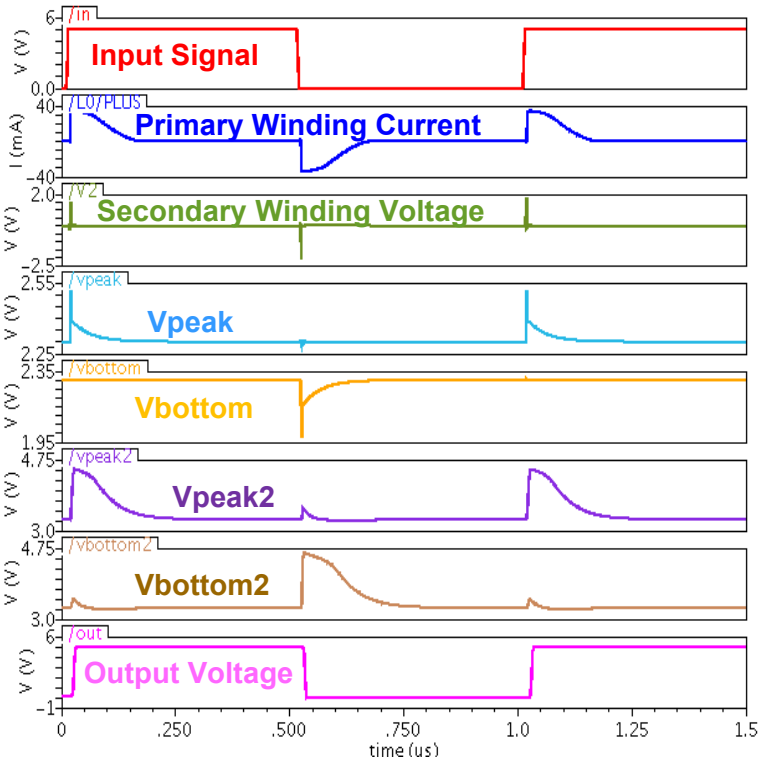
- In a phase-leg, overcurrent failure is a key issue:
  - Under normal operating mode, anti-cross talk circuitry mitigates noise induced potential shoot-through failure
  - Under short-circuit mode, desaturation protection prevents damage to the SiC MOSFETs due to large overcurrent

Technical Accomplishments and Progress – Input Isolation

- Full schematic and layout have been designed and simulated
- Simulations show functionality of isolation design
- Waveforms show functionality with 1 MHz input signal



Schematic of Input Isolation

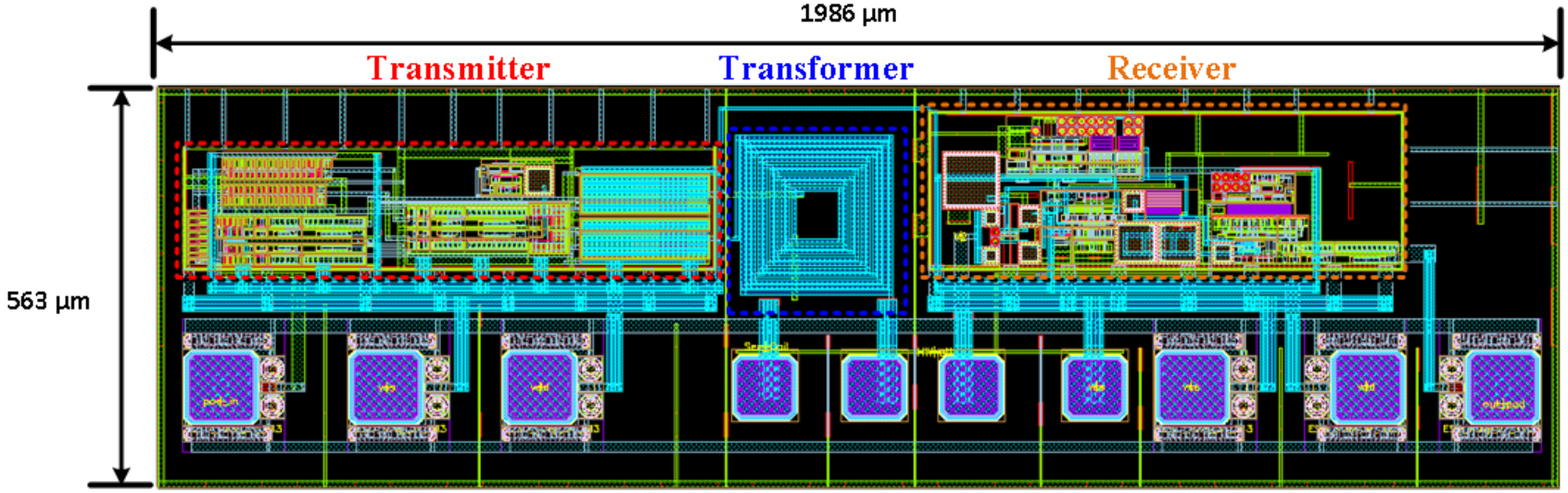


Simulation Waveforms

Technical Accomplishments and Progress – Input Isolation

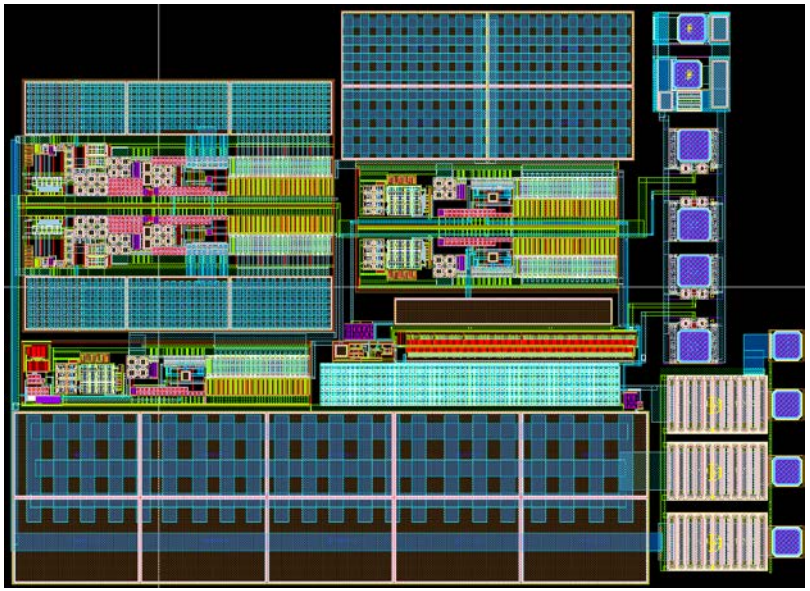
- Completed design of schematic and chip layout in SOI chip technology
- Prototype #1: (submitted for fabrication in March 2013) SOI process used for gate driver, best high temperature capability
- Prototype #2: (submitted for fabrication in April 2013) IBM process with more metal layers, improved isolation and transformer model

SOI Isolation Chip Layout



Technical Accomplishments and Progress – Power Supply on Chip (PSOC)

- Designed and simulated boost converter for power supply in package at temperatures up to 200 ºC
  - +20 V output voltage with < 5% ripple at 150 mA for 11 – 18 V input
- Submitted integrated circuit design of boost converter for power supply in package with a PCB-embedded inductor (March 2013)

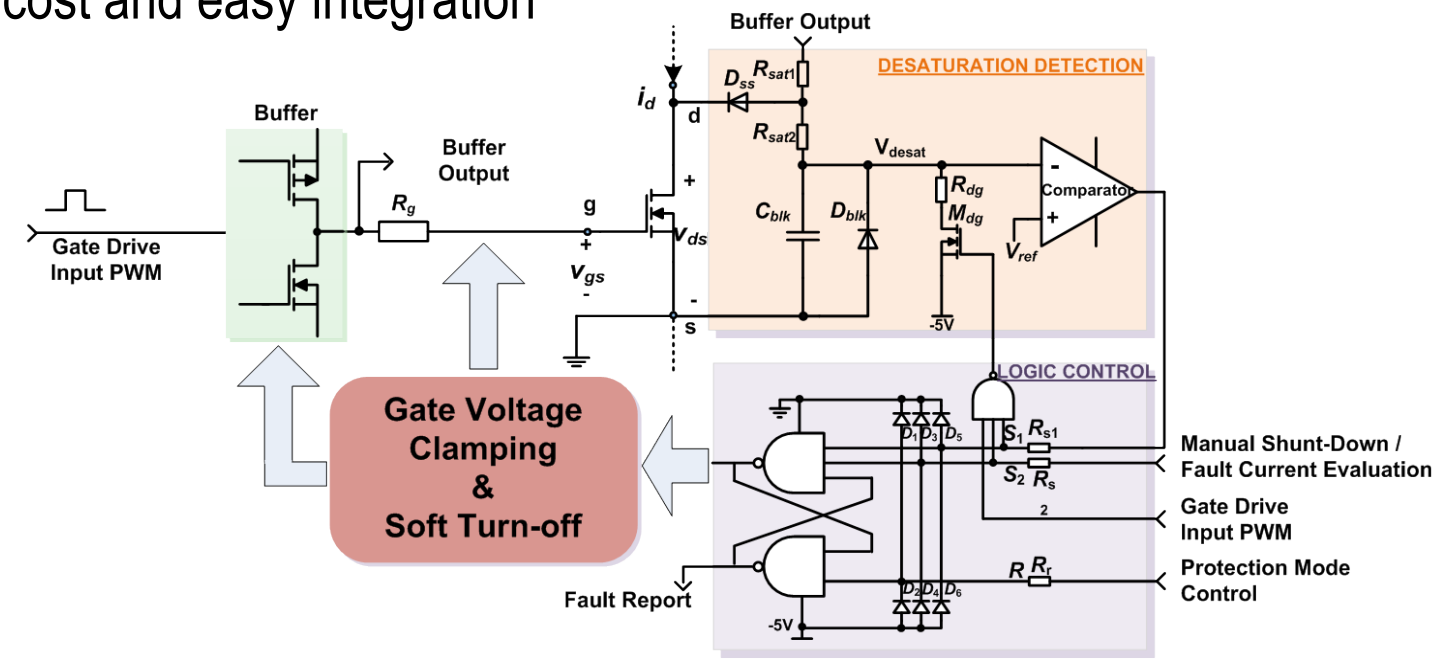


On-Chip Power Supply Layout

Technical Accomplishments and Progress - Overcurrent Protection

Developed protection circuit for SiC MOSFETs:

- Fast fault response time (< 200 ns)
- Flexible protection modes without interruption of converter operation in the event of momentary short circuits
- Low cost and easy integration

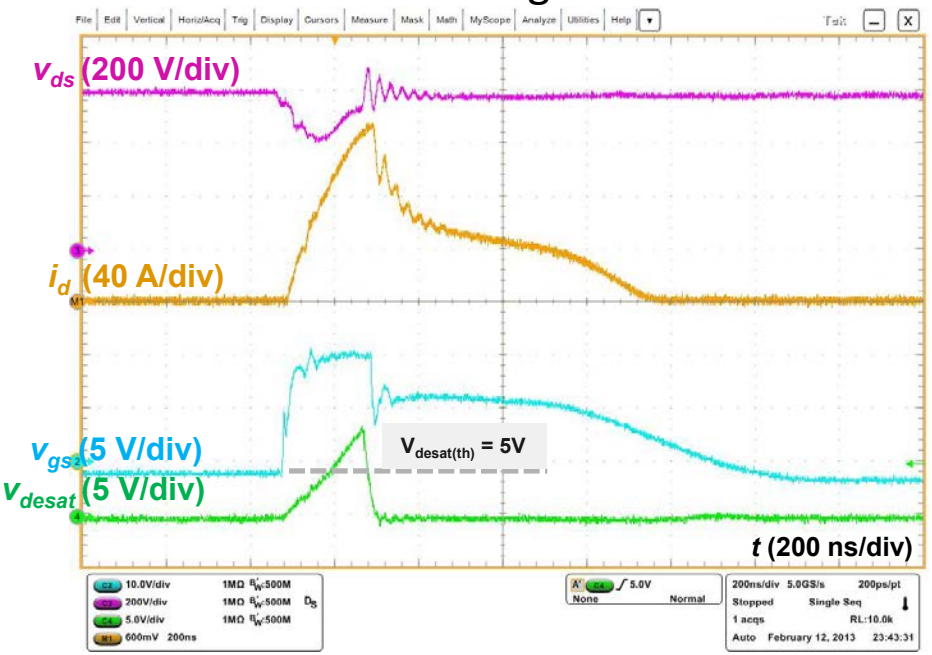


Proposed desaturation protection circuit

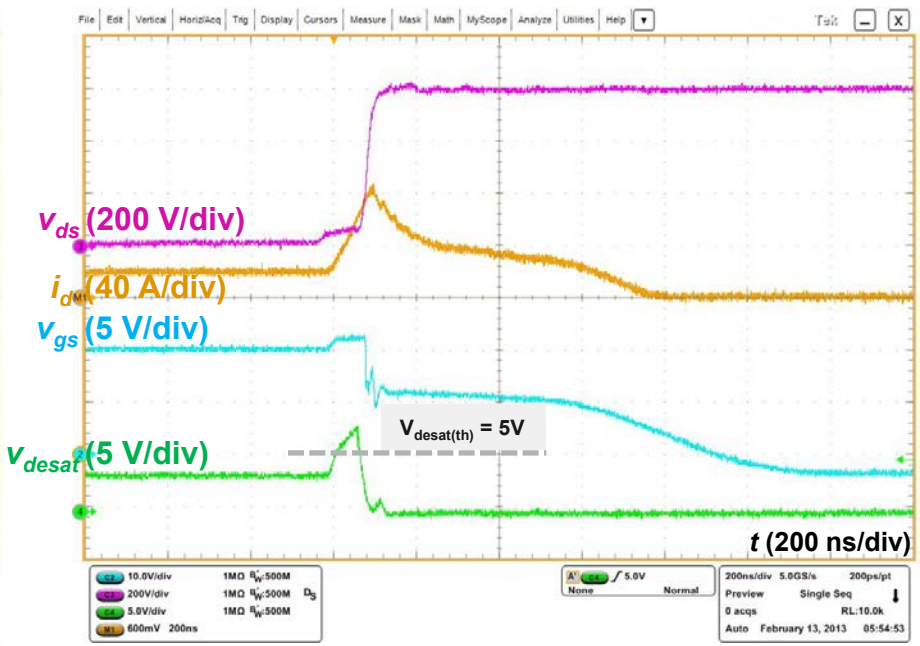
Technical Accomplishments and Progress - Short Circuit Protection Test Results

V_{dc}= 600 V; $V_{desat(th)}$ = 5 V; Blanking time = 100 ns

Hard Switching Fault



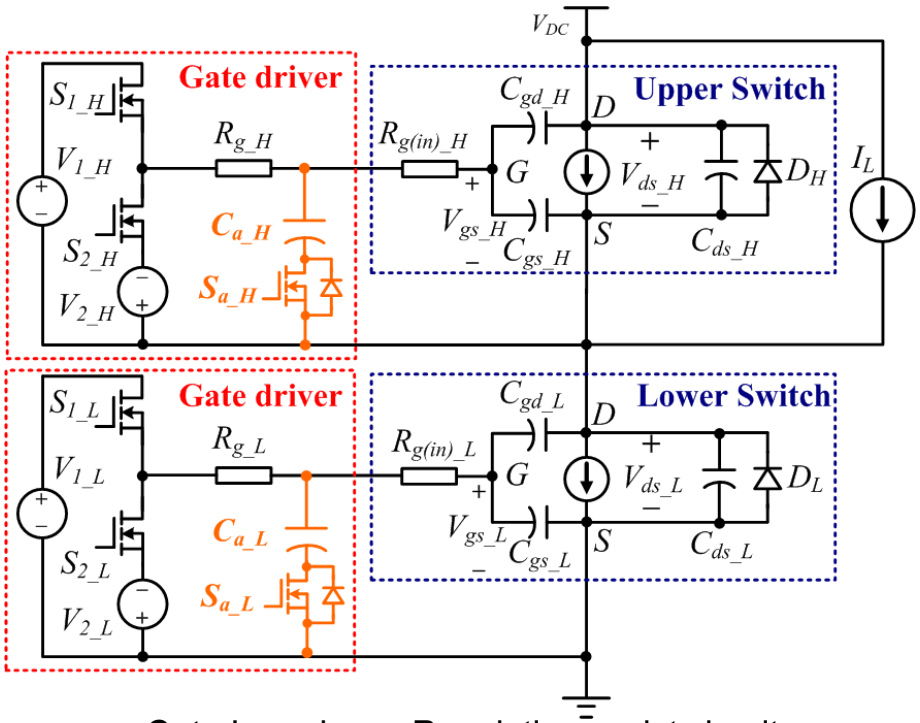
Fault Under Load



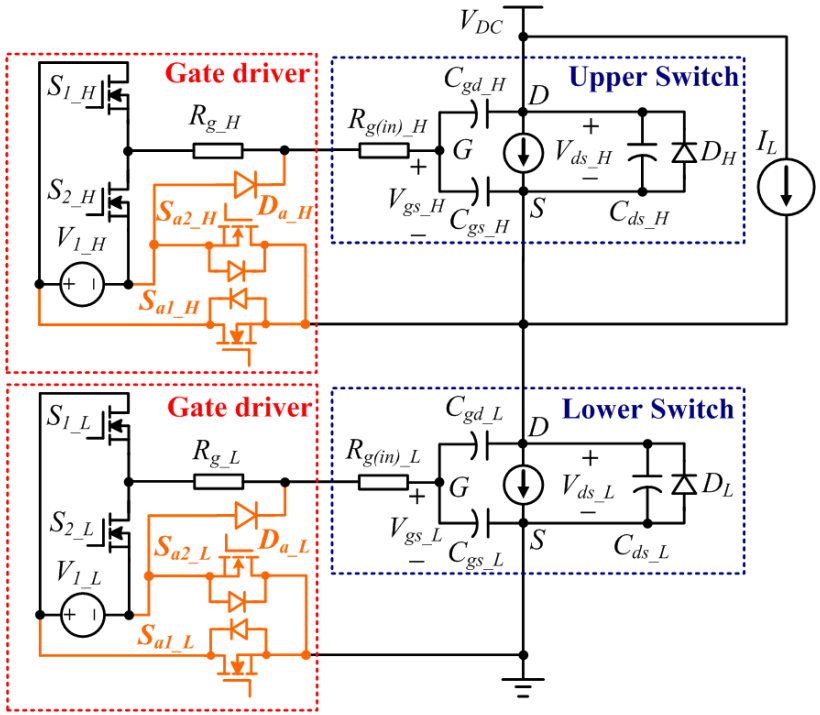
- ❑ Fault current is detected and limited within 200 ns
- ❑ Gate voltage v_{gs} is clamped to suppress the fault current level
- ❑ Soft turn-off is implemented to avoid large turn-off overvoltage

Technical Accomplishments and Progress - Gate Drive Circuit for Cross Talk Suppression

- Two gate assist circuits proposed for WBG-based phase leg:
  - Gate impedance regulation (GIR) assist circuit
    - — Fewer auxiliary components, suitable for board level integration
  - Gate voltage control (GVC) assist circuit
    - — All-transistor-based auxiliary components, suitable for chip level integration



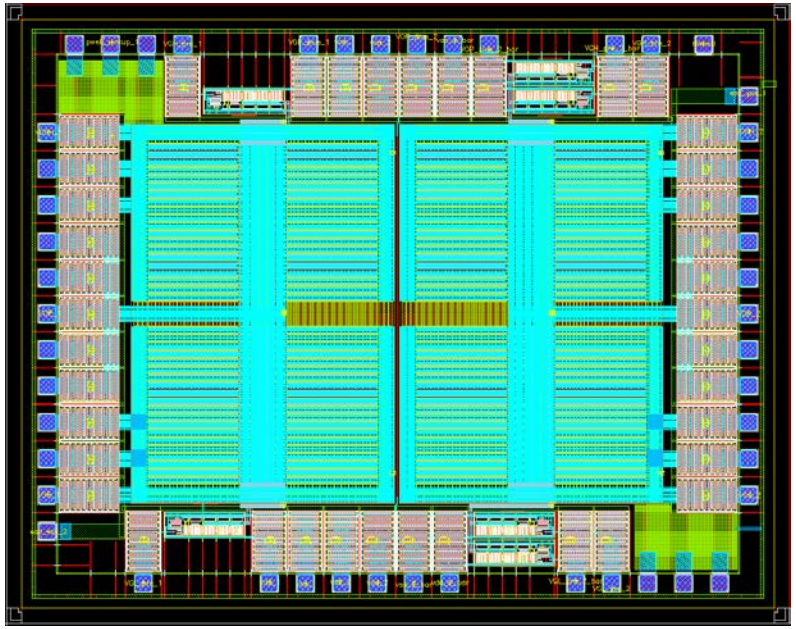
Gate Impedance Regulation assist circuit



Gate Voltage Control assist circuit

Technical Accomplishments and Progress – SOI Gate Drive

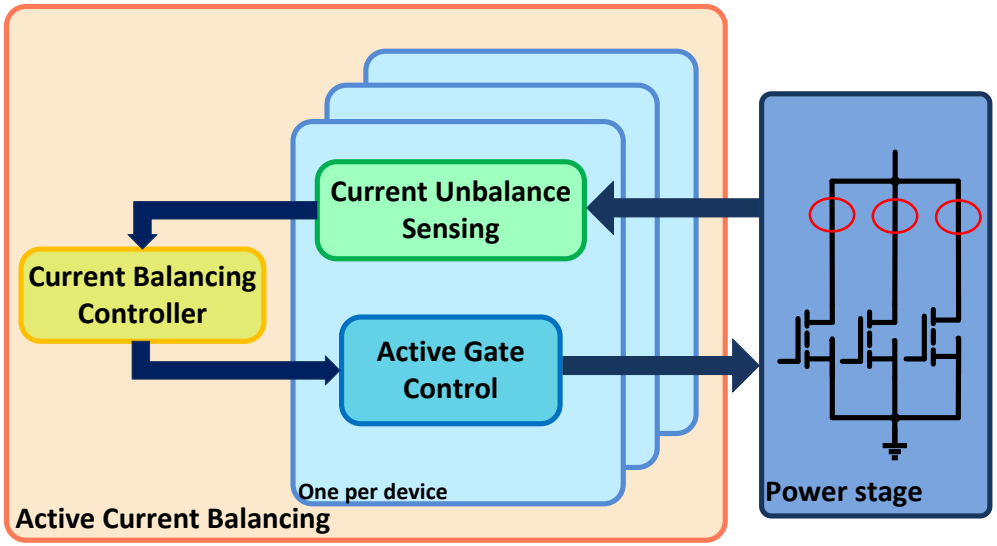
- **New SOI gate drive design revision is highly modular through the use of a multi-chip solution – chip design submitted for fabrication in March 2013**
  - Allows the end user flexibility in their design and use
- **New revision is made up of four individual chips**
  - Isolation
  - Voltage regulators and protection circuitry
  - Signal management
  - Output drivers
- **Can drive either single or paralleled WBG devices**
- **Can drive half or full bridge topology**
- **Allows the addition of an off-chip current buffer by providing *Vop* and */Vop***
- **Revision increases the robustness and lifetime of the gate drive**



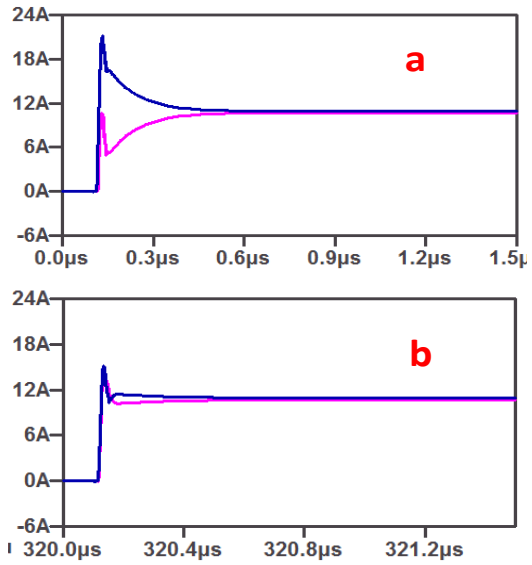
Dual Output Drivers

Technical Accomplishments and Progress –
Active Current Balancing for Parallel-Connected WBG Devices

- **An active current balancing (ACB) scheme for parallel SiC MOSFETs has been simulated.**
  - Current unbalance sensing: sense the unbalanced current in the devices
  - Current balancing controller: generates the correction needed based on the measured unbalance
  - Active gate control: vary the gate drive signal according to the signal from the balancing controller



Block diagram of the ACB scheme



Simulation results: drain currents of two mismatched parallel devices (a)without and (b)with ACB scheme

Collaboration and Coordination

Organization	Type of Collaboration/Coordination
The University of Tennessee	Highly integrated active gate drive and isolation structures
Institute National des Sciences Appliquées de Lyon (INSA - Lyon, France)	IC prototyping support and high-temperature device testing collaboration
CREE	Supply SiC MOSFETs and diodes
ORNL	High temperature packaging and testing

Proposed Future Work

- **Remainder of FY13**
  - Input isolation
    - SOI chip fabrication in March, receive for testing in May
    - IBM chip fabrication in April, receive for testing in June
    - Two chip designs will be tested for functionality and isolation capability
    - Make decision about continuing pursuit of full on-chip integration of isolation
  - Power supply on chip
    - Characterize on-chip inductor in designated process for use in power supply on chip
    - Test power supply in package board including boost converter chip and PCB inductor
  - Package gate drive chip and devices in a module

Proposed Future Work

- **FY14**
  - Input isolation
    - Pursue isolation with module substrate integrated transformer if isolation chips do not meet isolation requirements
      - Leverage previous work on PCB integrated transformers
    - Integrate final isolation solution with module packaging
  - Power supply on chip
    - Continue to modify switched-mode power supply design to allow for on-chip inductor
    - Design buck-boost converter for -2 V supply and buck converter for +5 V supply
  - Overcurrent protection
    - Integration of the developed active protection circuit into the power module together with the SOI gate driver and the power switches.

Proposed Future Work

- **FY14**
  - SOI gate drive
    - Fully integrate cross talk mitigation circuitry
    - Integrate desaturation protection
    - Place in a high-temperature module
  - Module layout design
    - Evaluation of the impact of parasitics on switching behavior of power devices in a phase-leg configuration
    - Development of guidelines for optimal layout design of phase-leg power module
  - Active current balancing for parallel-connected devices
    - Implement the active current balancing scheme on multiple power switches

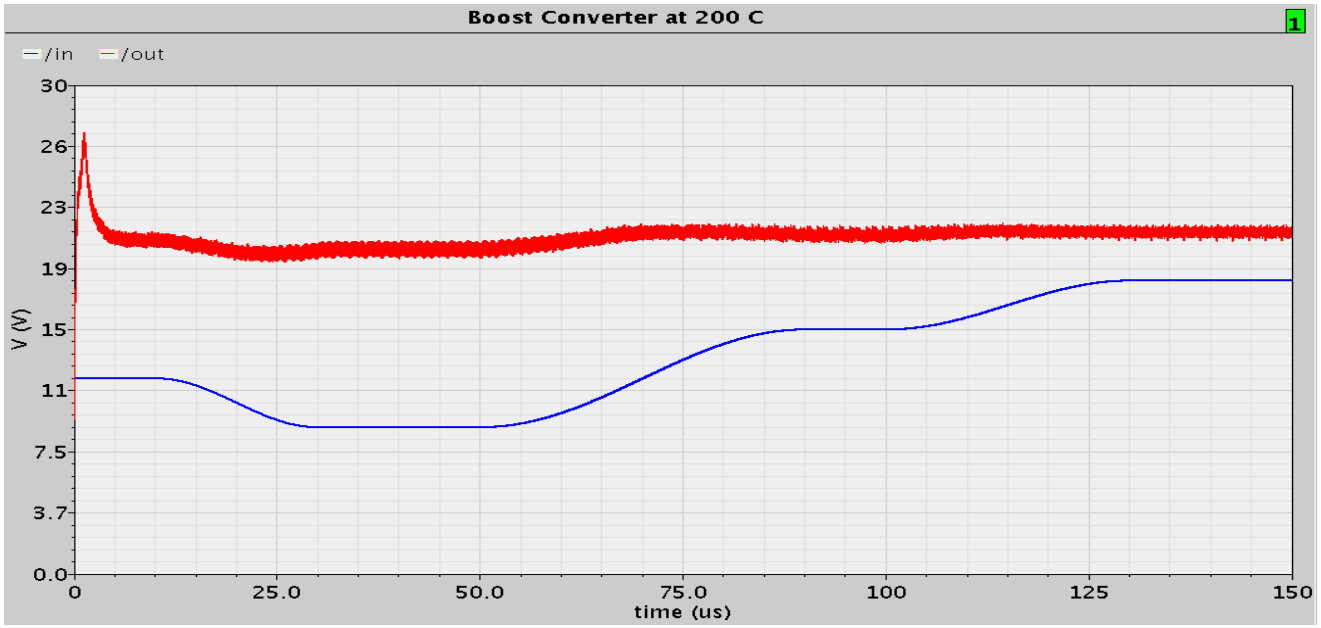
Summary

- Relevance: This project will develop a highly integrated power module incorporating WBG power electronic devices to reduce power density and cooling requirements by using high temperature packaging and components.
- Approach: Develop a highly integrated power module phase leg (rated at 1200 V and 200 A) incorporating wide bandgap devices that includes: (1) an integrated gate drive, (2) isolation chip, and (3) power supply on a chip, and (4) special protection features to enable fast switching of WBG devices.
- Collaborations: Working with universities in U.S. and France on high temperature gate drive and protection circuitry and with U.S. industry in using their WBG devices.
- Technical Accomplishments: Designs have been developed and submitted for fabrication for isolation chip, new gate drive chips, protection circuitry, PSOC.
- Future Work: Fabricated individual chips will be tested and characterized later in FY13. Initial high temperature packages will be fabricated in FY13. Chip designs will be refined and integrated into a high temperature package in FY14.

Technical Back-Up Slides

Technical Back-Up – Power Supply

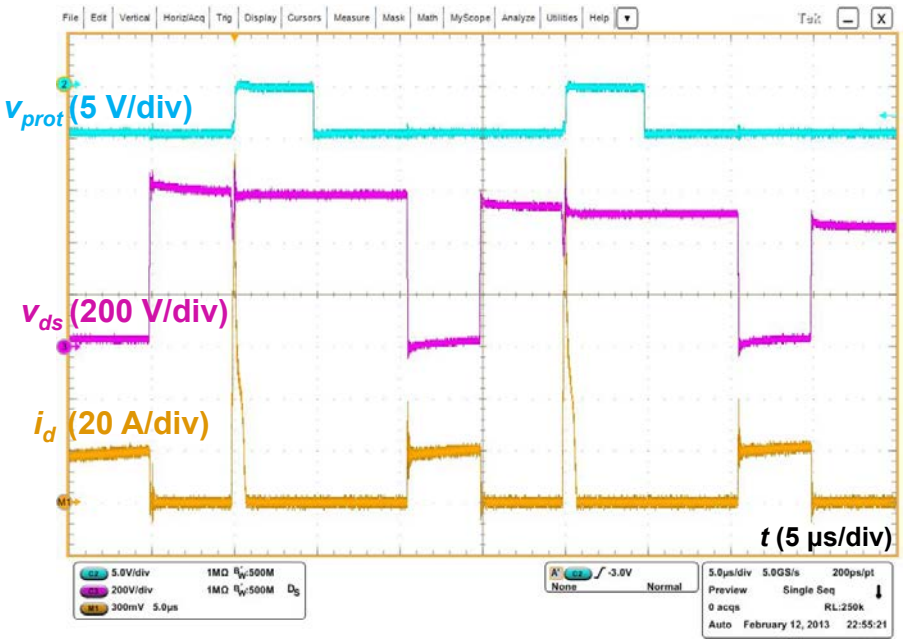
- Simulation results of boost converter for +20 V supply at 200 °C
  - 50 MHz switching frequency
  - 125 mA output current
  - PCB embedded 400 nH inductor with ~ 1 Ω series resistance



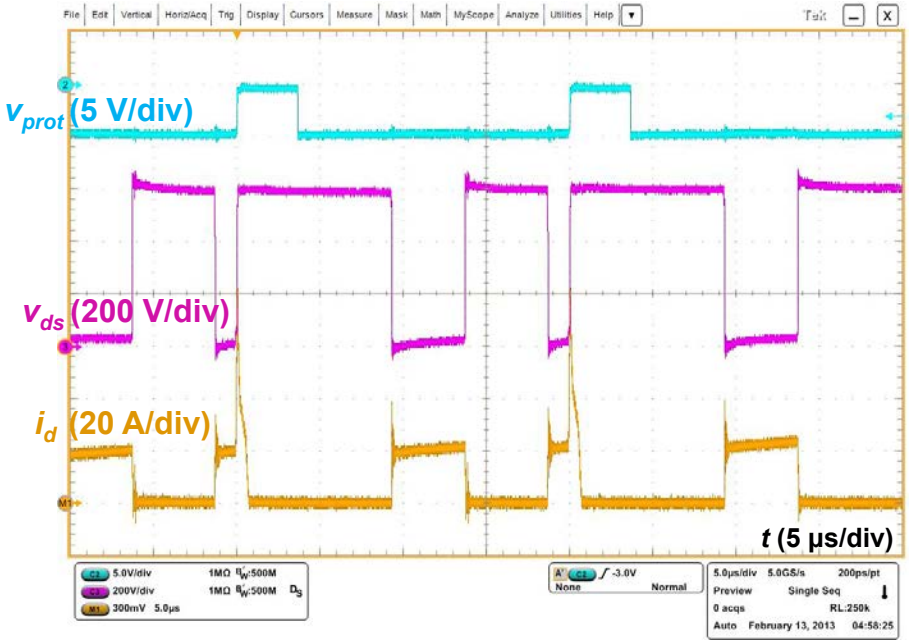
Technical Back-Up - Short Circuit Protection

V_{dc}=600V; $V_{desat(th)}$ = 5V; Blanking time = 100 ns; Multiple Mode

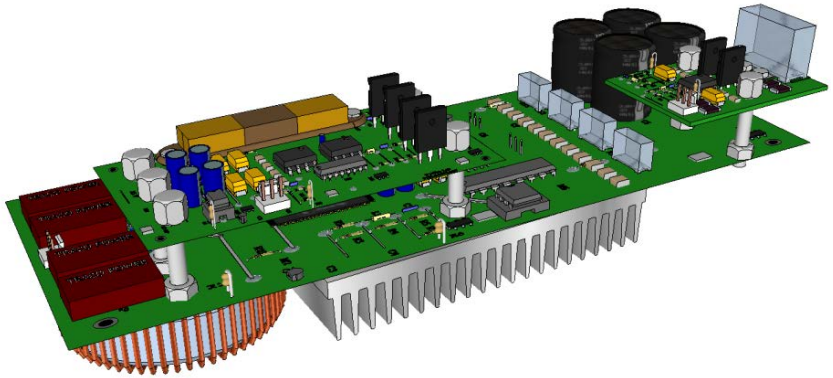
Hard Switching Fault



Fault Under Load

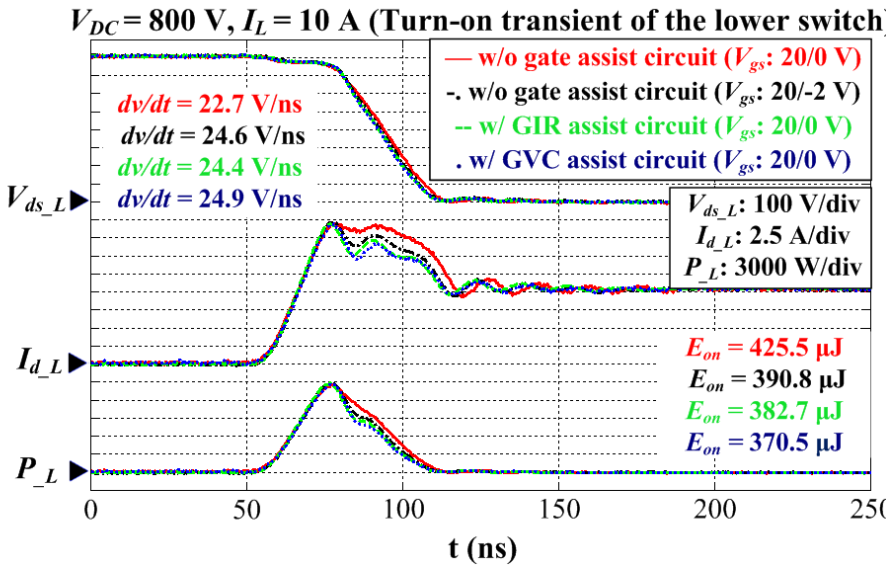


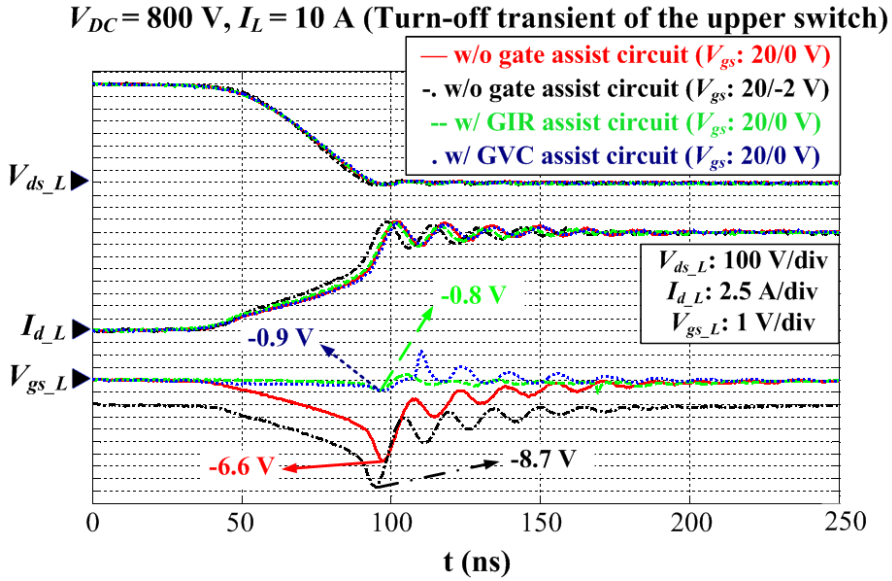
Multiple Mode: Gate driver will only be blocked in the fault switching cycle, and continues to work until a shutdown signal is sent by a microprocessor counting the reported fault times.



Hardware testbed for SiC MOSFET protection

Technical Back-Up - Gate Drive Circuit for Cross Talk Suppression



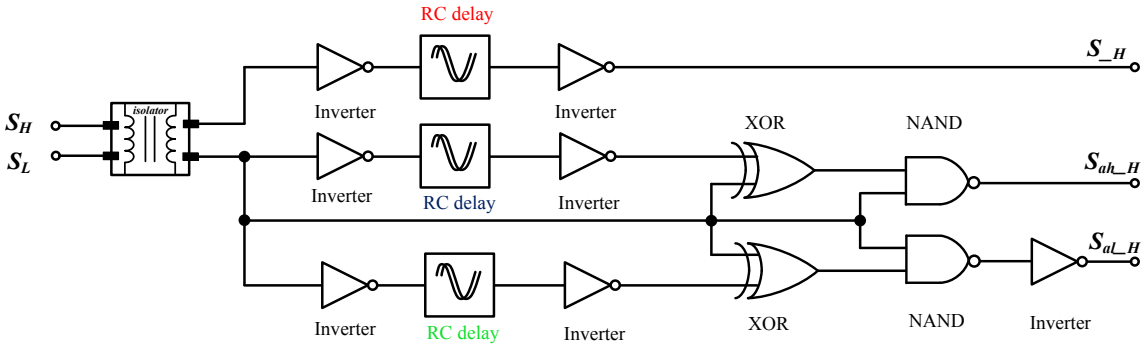


* GIR: gate impedance regulation. GVC: gate voltage control.

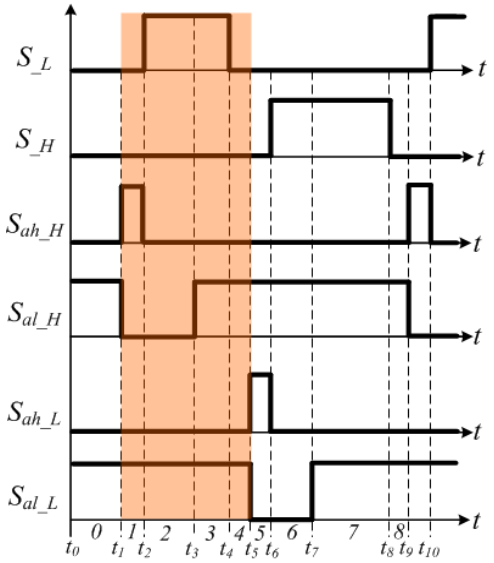
- **Two anti-cross talk circuitries have developed, enabling:**
  - Turn-on energy loss reduction of more than 17%
  - *dv/dt* improvement during turn-on switching transition
  - Reliability of devices enhancement (spurious negative gate voltage minimization within the required range)

Technical Back-Up – SOI Gate Drive

- Contains logic synthesis to produce the necessary waveforms for the cross talk mitigation circuitry



RC delay: determined by propagation delay of logic gates (~50 ns);
RC delay: determined by pre-charge interval (~20ns for CREE SiC MOSFETs);
RC delay: determined by switching time (~200ns for CREE SiC MOSFETs).



Technical Back-Up - Active Current Balancing for Parallel-Connected WBG Devices

Developed active gate control circuit:

- Dynamic current unbalance can be eliminated by proper control of the gate signal delay.
- A variable gate delay circuit is proposed for parallel SiC MOSFETs.
  - Delay is continuously adjustable by $V_{control}$.
  - Low circuit complexity and cost.
  - All the parallel devices can share one gate driver.