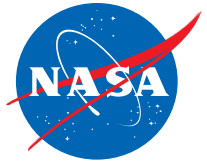


Development of SiC Large Tapered Crystal Growth

Principle Investigator: Philip G. Neudeck

NASA Glenn Research Center

Presenting Co-Investigator: Andrew J. Trunek

OAI

Project ID #
APE027

June 10, 2010

Overview

SiC Large Tapered Crystal Growth

Timeline

- Funding start: Dec. 2009
- Project end: Dec. 2011
- Percent complete: 20%

Budget

- Total project funding
  - DoE: $1200K
  - NASA: $180K
- Funds received FY09: $0
- Funds received FY10: $700K

Barriers

- Advanced Power Electronics and Electric Machines (APEEM)

SiC expense and material quality inhibiting higher density and higher efficiency EV power electronics.

Table 1. Technical Targets for Electric Traction System

	2020[b]
Cost, $/kW	<8
Specific power, kW/kg	>1.4
Power density, kW/L	>4.0
Efficiency	>94%

Partners

- NASA Glenn Research Center
- Ohio Aerospace Institute
- Sest, Inc.
- Oak Ridge Assoc. Universities

Objectives

- SiC power semiconductor devices should theoretically enable vastly improved power conversion electronics compared to today's silicon-based electronics.
  - 2-4X converter size reduction and/or 2X conversion loss reduction (theoretical performance gains vary with system design specifications).
  - Fundamentally improved implementation of smart grid, renewable energy, electric vehicles, aircraft and space power systems.
- SiC wafer defects and cost inherent to existing material growth approach presently inhibiting large benefits from becoming widely & reliably available.
- New but unproven NASA "Large Tapered Crystal" SiC growth concept proposed to remove SiC material technology barrier.

Graphical illustration of power converter size reduction modeled by using SiC devices instead of silicon power devices.

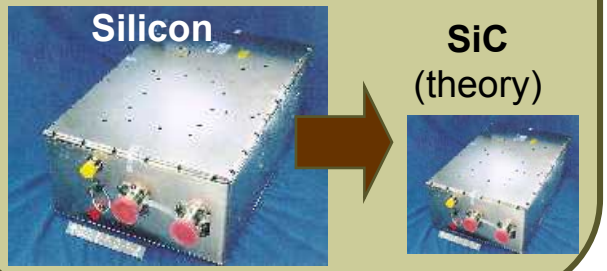


Table 3.2-7. *Proposed APEEM Targets for Advanced Hybrid and Fuel Cell Vehicles*

Parameter	2010 Target	2015 Target	2020 Target
Integrated Electric Propulsion System (Traction Motor and Power Electronics Inverter/Controller)			
Power Level, peak/continuous, kW	55/30	55/30[a]	55/30[a]
Specific Power at Peak Load, kW/kg	>1.06	>1.2	>1.4
Volume Power Density, kW/L	>2.60	>3.5	>4.0
Cost, $/kW	<19	<12	<8
Efficiency 10% to 100% speed, 20% rated torque	>90	>93	>94
Coolant Temperature, °C	90	105	105
DC/DC Converter (approx 5 kW) and Transmission			
Specific Power at Peak Load, kW/kg	0.8	>1.0	>1.2
Volume Power Density, kW/l	1.0	>2.0	>3.0
Cost, $/kW	75	<50	<25
Efficiency 10% to 100% speed, FTP drive cycle	93	95	96
Coolant Temperature, °C	90	105	105

[a] *Fuel cell vehicle power requirements may be higher than 55/30 kW; however, it is deemed easier to scale up to specific vehicle requirements and still meet cost and performance targets.*

Objectives

FACT: Majority of large benefits (of significantly higher efficiency and power density) theoretically enabled by wide bandgap semiconductor (e.g., SiC and GaN) power devices to power systems (including electric/hybrid vehicles) have **not** been realized/commercialized.

High cost and high dislocation defect density of starting SiC & GaN wafer material are widely recognized as major inhibitors to realizing wide bandgap power devices for large system benefits.

Overall Objectives

- Open a new technology path to large-diameter SiC and GaN wafers with **1000-fold dislocation defect density improvement at 2-4 fold lower cost.**
- Enable leapfrog improvement in wide band gap power device capability and cost to in turn enable leapfrog improvements in electric power system performance (higher efficiency, smaller system size).

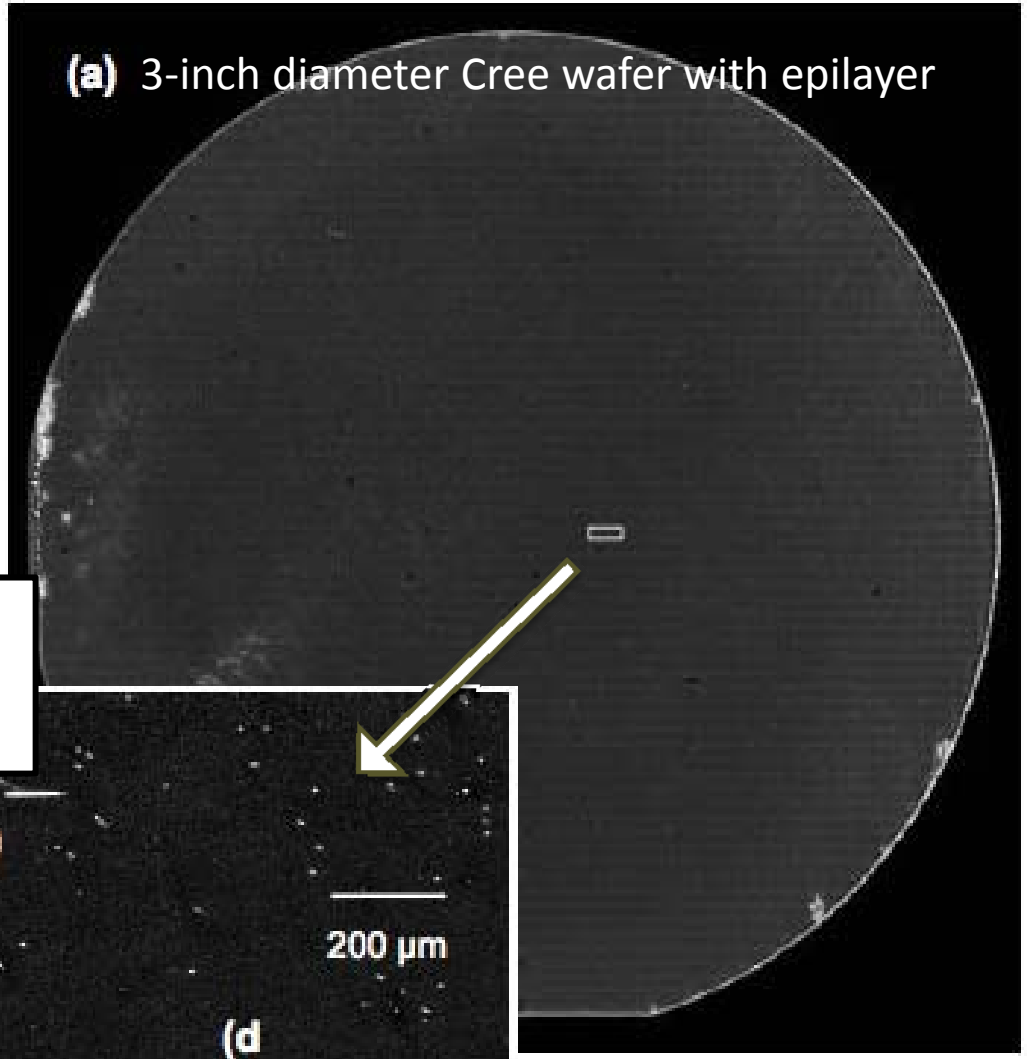
Funded 2-Year Project Objective

- Demonstrate initial feasibility of radically new “Large Tapered Crystal” (LTC) approach for growing vastly improved large-diameter SiC semiconductor wafers.

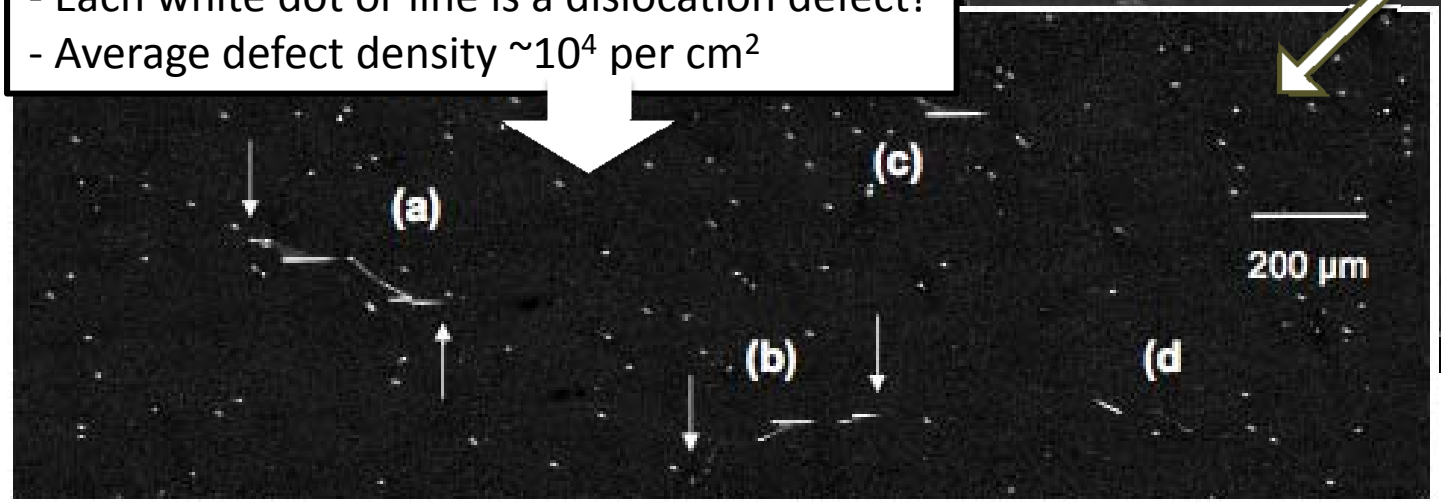
Approach/Strategy

Dislocation Defects in 4H-SiC Commercial Wafers

Over the past decade there have been numerous publications (including NASA Glenn studies) linking degraded SiC power device performance, yield, and reliability to the presence of dislocation defects in the SiC wafer crystal.



Magnified view small area in middle of wafer
- Each white dot or line is a dislocation defect!
- Average defect density ~10^4 per cm^2

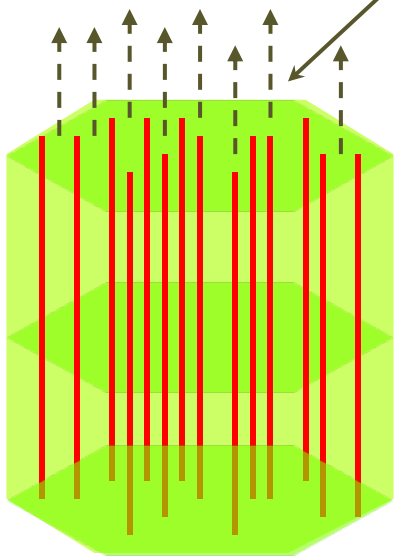


Dislocation mapping images from Stahlbush et al, Mat. Sci. Forum vol. 556-557, p. 295-298 (2007)
- Ultra-Violet Photoluminescence Imaging (UVPL) dislocation imaging technique shown.

Approach/Strategy

Commercial SiC Wafer Growth Approach

(Sublimation growth or High Temperature CVD)



C-axis (vertical) growth proceeds from top surface of large-area seed crystal via thousands of screw dislocations.

Vertical growth rate would not be commercially viable (i.e., would not be high enough) without high density (> 100 cm^{-2}) of screw dislocations.

Crystal enlargement is vertical (up c-axis).
Negligible lateral enlargement.

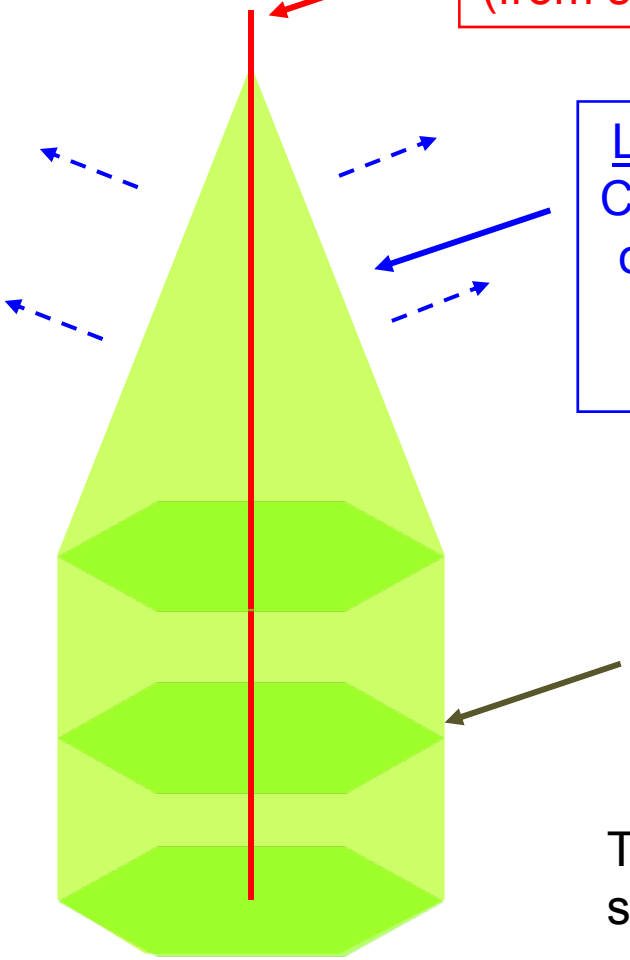
Thermal gradient driven growth at T > 2200 °C
High thermal stress/strain

Fundamental Flaw: Abundant screw dislocation defects are needed for present SiC wafer growth approach, yet these same defects harm SiC power device yield and performance (cause blocking voltage de-rating, leakage, etc.).
- High thermal stress also generates dislocations.

Approach/Strategy

New Approach - Large Tapered Crystal (LTC) Growth

(US Patent 7,449,065 Owned by OAI, Sest, Inc., with NASA Rights)



Vertical Growth Process:
Fiber-like growth of small-diameter columnar tip region (from single screw dislocation)

Small-diameter c-axis fiber from single screw dislocation at mm/hour rate.

Lateral Growth Process:
CVD growth enlargement on sidewalls to produce large-diameter boule (T = 1500 - 2000 °C)

MOST of crystal grown via epitaxy process on laterally expanding taper **at significantly lower** growth temperature **(lower thermal stress)** and growth rate.

Completed boule section
Ready for slicing into wafers

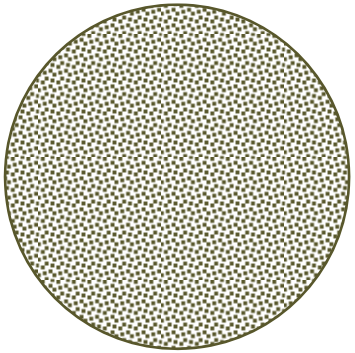
Large diameter wafers yielded at mm/hour (wafers/hour) growth rate!

Tapered portion is then re-loaded into growth system as seed for subsequent boule growth cycle.

Approach/Strategy

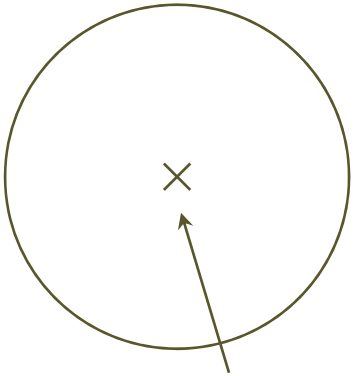
LTC Vision: Dramatically improved SiC wafer quality realized at higher volumes and lower production cost.

Present-Day SiC Wafer



~1,000-10,000 screw dislocations/cm^2
< 0.5 wafers per hour
Cost: > $2000/4-inch wafer
Commercial Power Devices
Limited to < 50-amp/die, ~1 kV

LTC SiC Wafer



Ideally ~1 screw dislocation/cm^2
> 1 wafer per hour
Cost: ~ $500/6-inch wafer
Commercial Power Devices
100-1000-amp/die, > 10kV

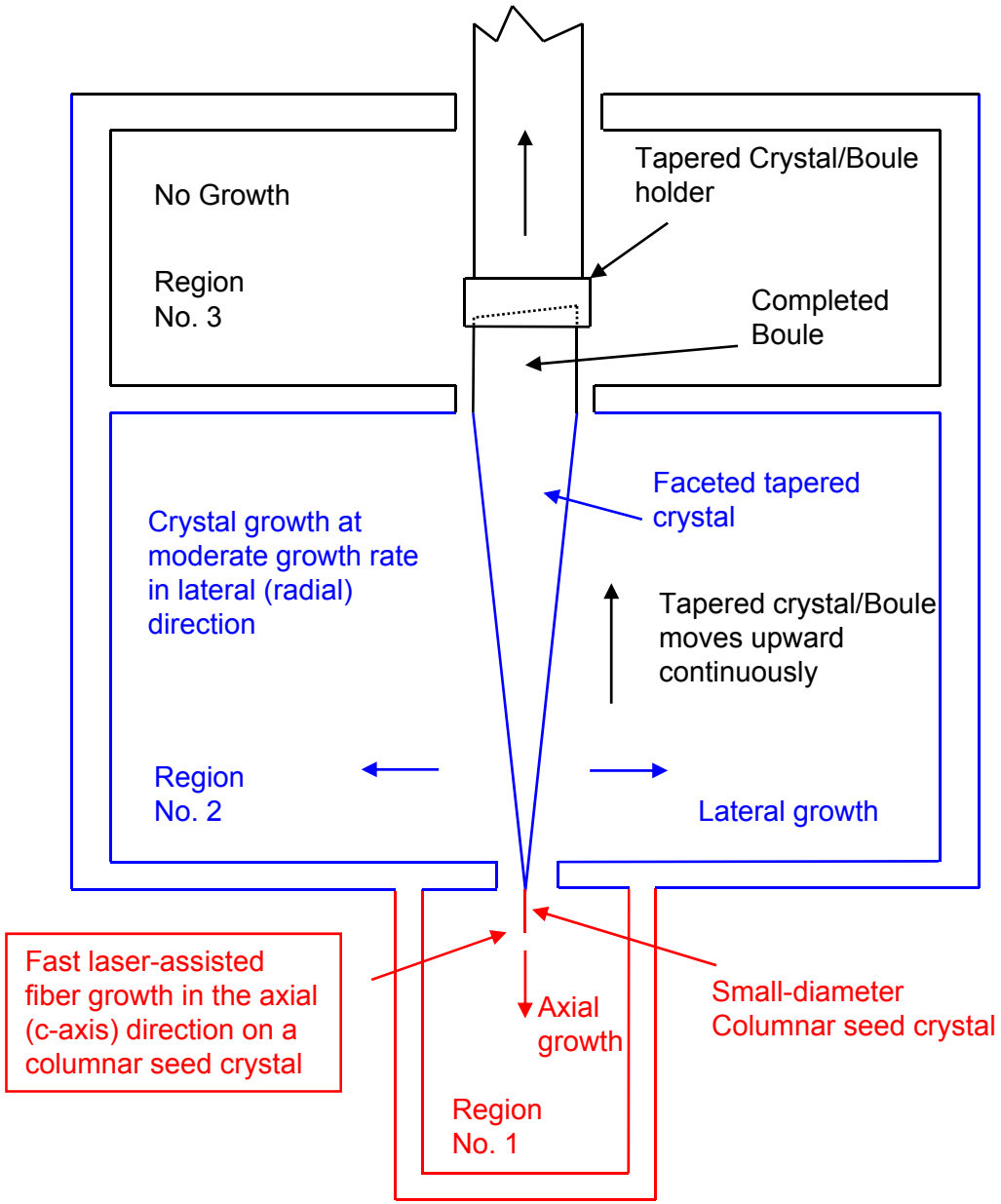
Drastic wafer improvement sufficient to unlock full SiC power device potential.
(Approach also applicable to 3C-SiC, GaN, Diamond, and other semiconductors)

However, LTC growth process is totally new and unproven. This work seeks to experimentally investigate fundamental feasibility of LTC growth approach in SiC.

Approach/Strategy

Large Tapered Crystal (LTC) Growth Method

Simplified Schematic Cross-Sectional Representation



Features (one embodiment):

1. **3-Region growth apparatus for 3 different growth actions.**
2. **Region 1: Vertical (c-axis) growth on a very small diameter columnar portion ("Fiber Growth" Year 2 Milestone).**
3. **Region 2: Lateral (m-direction) growth on fiber & tapered portion ("Lateral Growth" Year 1 Milestone).**
4. **Region 3: No growth after LTC boule reaches desired diameter.**
5. **Growth rate of boule in c-axis direction equals fast growth rate of columnar seed crystal.**
6. **Boule contains only one dislocation along its axis; the remainder of the boule is nominally defect-free.**

Approach/Strategy

Comparison of LTC with Current State of the Art

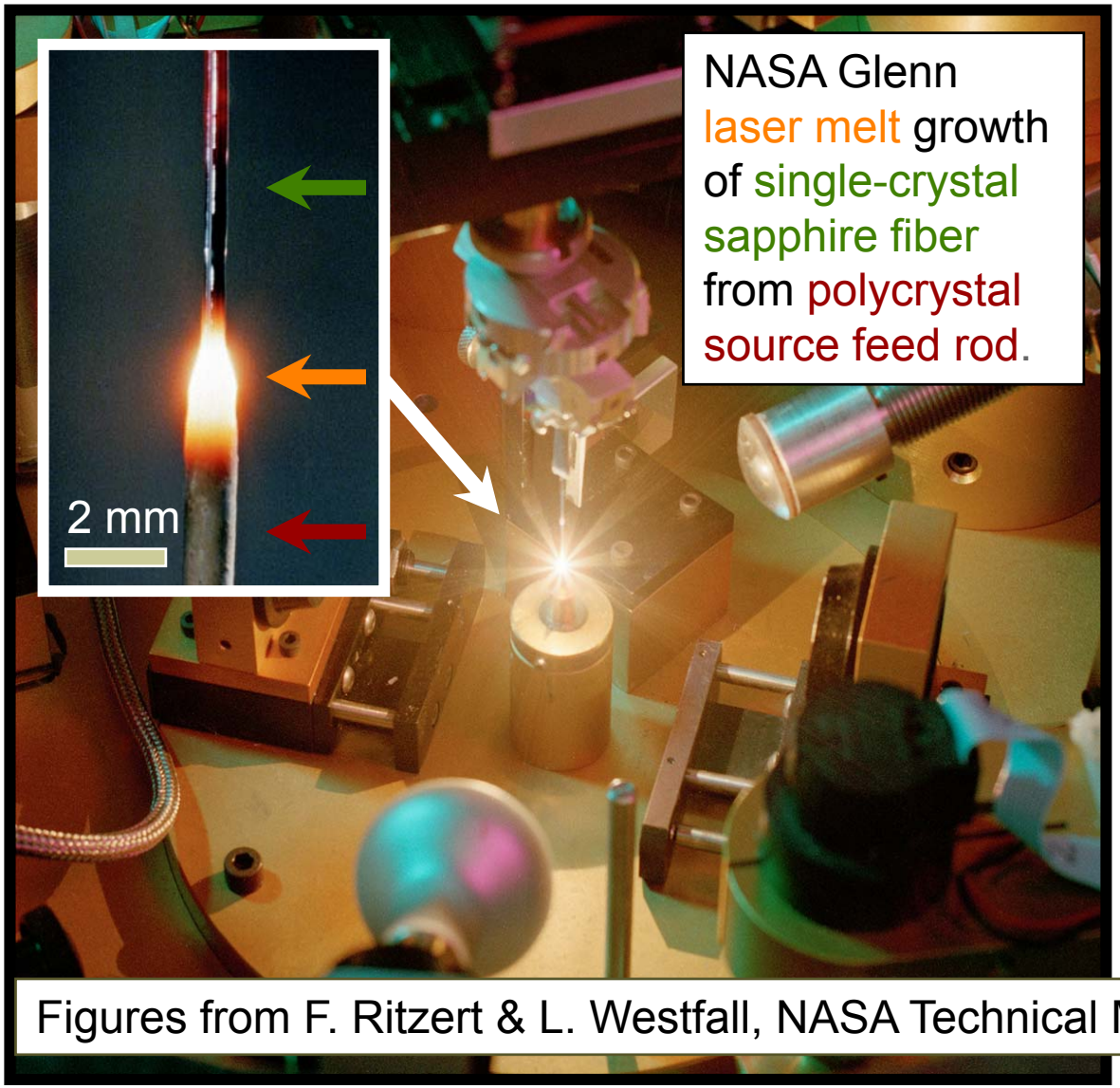
Large Tapered Crystal (LTC) SiC	Current SiC Boule Growth
Boule thickness enlargement at ~mm/hour	Boule thickness enlargement at ~mm/hour
Wafer contains only one threading screw dislocation (TSD) - Known location in middle of wafer	**Wafer contains many thousands of TSDs (100s to 10,000s per cm^2 densities)** - BPD multiplication via TSD climb [1]
Boule grown via CVD epi at 1400-1900 °C **- Nearly isothermal deposition** **- Lower thermal stress** (minimal stress-induced dislocations)	**Boule grown at > 2200 °C** **- Temperature gradient driven deposition** **- High thermal stress** (abundant stress-induced dislocations)
Wafer itself can serve as lightly-doped high-voltage blocking layer - Eliminates need for thick SiC epilayer	**Wafer cannot be used as blocking layer** - Thick SiC epilayer must be grown on top of wafer to provide high-voltage blocking layer
Rapid wafer diameter up-scaling - Diameter set by growth system geometry	Wafer diameter up-scaling slower via repeated progressive seed crystal enlargement growths
No waste from off-axis wafer cut (optimal wafer off-angles at no loss/cost)	Part of boule wasted by off-axis wafer cut (% lost increases with diameter & off-angle)
Isothermal holding chamber enables production of much thicker SiC boules	Reactor & source charge degradation, T gradients/profile limit SiC boule thickness
Higher device performance and yield	De-rated device performance and low yield

[1] BPD = Basal Plane Dislocation - See Chen et al., Mat. Res. Soc. Proc. vol. 911 p. 151 (2006)

Approach/Strategy

Build on NASA Glenn pioneering expertise and facility for growing long (> 10 cm) high-quality single-crystal fibers via high temperature laser-assisted growth.

- Decade of laser fiber-growth experience for variety of single-crystal oxides.
- Modified argon-atmosphere chamber needed SiC growth of LTC fiber.



Build on SiC melt solvent alloy growth chemistries already demonstrated for SiC growth.
- **Traveling Solvent (TS) [1]**
- Vapor-Liquid-Solid (VLS) [2]
- Si, C, and solvent (Ge, Fe, Cr, etc.) provided in source material feed rod.

Seed growth using small 4H-SiC mesa with screw dislocation.

[1] L. Griffiths et al., J. Electrochem. Soc., **111**, p. 805 (1964).
[2] W. Knippenberg et al., U.S. Patent 4,013,503, March 22, 1977.

Figures from F. Ritzert & L. Westfall, NASA Technical Memorandum 4732 (1996).

Milestones

First SiC experimental demonstrations of the two critical growth actions required for Large Tapered Crystal (LTC) process.

- Year 1 (FY10 – "Lateral Growth"): Demonstrate epitaxial radial growth of a 5 mm diameter boule starting from a simulated SiC fiber crystal.

- Year 2 (FY11 – "Fiber Growth"): Demonstrate laser-assisted fiber growth of a SiC fiber crystal greater than 10 cm in length.

LTC is **NOT** viable without success of BOTH milestones.

Note that throughout this presentation, issues related to "Lateral Growth" milestone are highlighted in blue, while issues relating to "Fiber Growth" milestone are all highlighted in red.

Technical Accomplishments and Progress

Majority of progress since project funding initiated in December of 2009 has been design and procurements for modification/build-up of laboratory hardware needed to initiate LTC experiments.

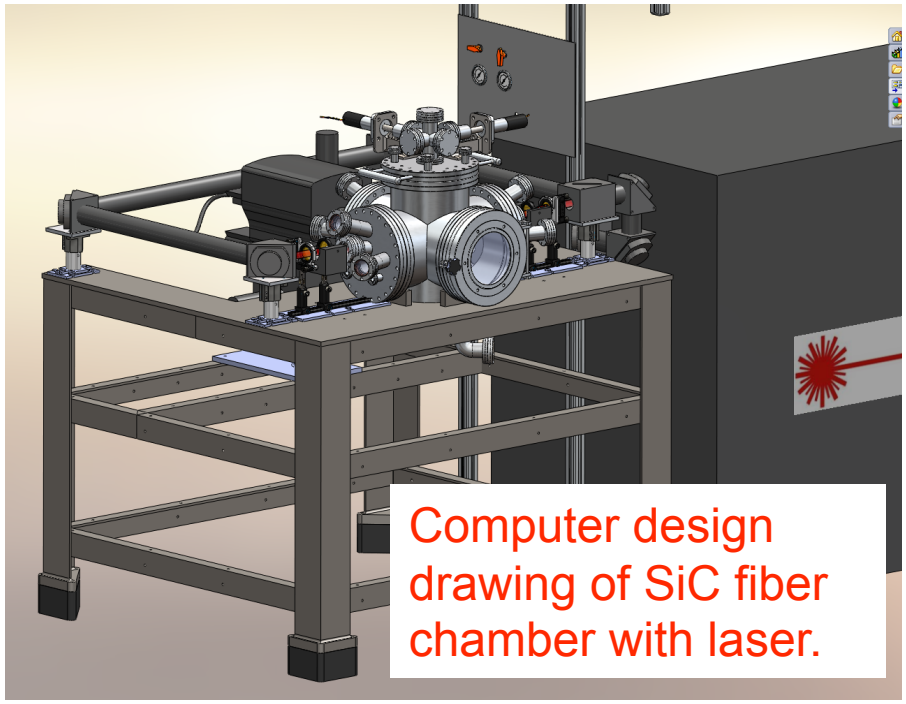
- **"Lateral growth"** and **"Fiber growth"** processes to be separately implemented in this project, each in its own dedicated laboratory.
  - "Lateral growth" to be carried out with modifications to existing SiC Growth Reactor #2 in NASA Glenn Aixtron Growth System in Building 77 Laboratory.
  - "Fiber growth" to be carried out with build-up of newly-designed and dedicated SiC laser-growth chamber in existing NASA Glenn Laser-Assisted Fiber Growth Laboratory in Building 106.

Project is new start (12/2009), so no previously reported accomplishments aside from patent, existing facilities and vast experience in technical field.

Following poster panels give further non-proprietary information about work in each lab. (Note that further details are contractor proprietary.)

Technical Accomplishments and Progress

Laser-Assisted SiC Fiber Growth Apparatus Design & Buildup



Computer design drawing of SiC fiber chamber with laser.

CAD Drawing by Mark Dieringer

Procured components by CO_2 laser for assembly.

Details

- Majority of base component procurements complete – assembly to begin in spring after key deliveries.
- Ultra-high vacuum (UHV) chamber which can be evacuated to remove contaminates (e.g., O_2 and H_2O).
  - Gas handling system to flow ultra-high purity Ar during growth.
- Growth process and data collection will be automated to precisely control and record conditions.
  - Detailed imaging of hot zone.
  - Precision fiber/seed positioning.
- ZnSe optics and windows will be used to handle the laser beam's wavelength and power.
- High power CO_2 laser has been serviced and ready for use – lab utility upgrades nearing completion.

Technical Accomplishments and Progress

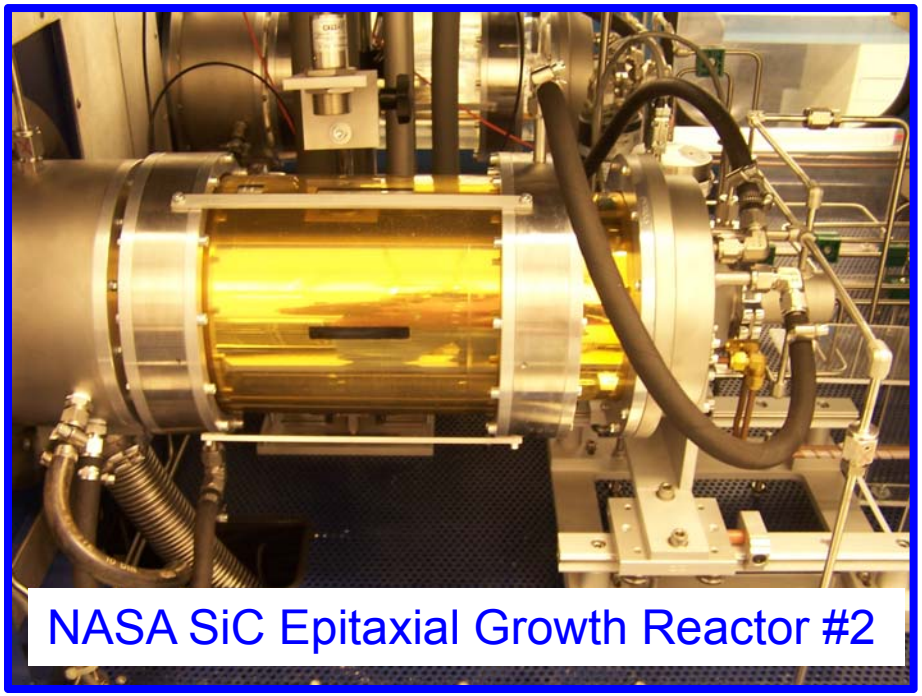
SiC Epitaxy Laboratory Upgrades for “Lateral Growth” Experiments

Preparations on-going for re-configuring SiC Epitaxy Reactor #2 for LTC work.

- Conversion from cold-wall to hot-wall reactor configuration.
- Conversion from full SiC wafer to SiC fiber sample mounting.
- Procurements and machining work underway.

Simulated SiC fiber seed crystals (cut from SiC boules) have been purchased and are being further prepared (etched & characterized) for upcoming lateral growth experiments.

NASA Aixtron SiC Growth System



NASA SiC Epitaxial Growth Reactor #2

Proposed Future Work

- Complete modifications of SiC epitaxial growth system to support radial (lateral) epi-growth of SiC fibers into boules.
- Carry out radial epitaxial growth of increasing diameter SiC boules starting from pseudo-fiber SiC seed crystals. **Achieve 5 mm diameter boule for Year 1 (FY10) Milestone.**

- Complete procurement and build-up of laser-assisted SiC fiber growth system and initiate first laser-assisted SiC fiber growth experiments.
- Carry out seeded laser-assisted growth of SiC fiber crystals of increasing length and quality. **Achieve 10 cm SiC fiber for Year 2 (FY11) Milestone.**

- Carry out extended defect characterization of crystals.
- Thermal modeling support of experiments/setups.

Collaboration and Coordination with Other Institutions

- NASA Glenn Research Center (Prime – 2 Research Organizations)
  - Sensors & Electronics Branch (RHS) – "Lateral Growth"
    - Two decades of SiC epitaxial crystal growth experience.
  - Ceramics Branch (RXC) – "Fiber Growth"
    - Decade of laser-assisted ceramic fiber growth experience.

- Ohio Aerospace Institute (Non-Profit Research Contractor)
  - Co-owner of core Large Tapered Crystal growth patent.
  - Dedicated Technical Lead on SiC Epitaxy (RHS Laboratory).

- Sest, Inc. (Industry Contractor)
  - Co-owner of core Large Tapered Crystal growth patent.
  - SiC Crystal Characterization Lead, Thermal modeling.

- Oak Ridge Assoc. Universities (University Post-Doc. Contractor)
  - Dedicated Technical Lead on Fiber Growth (RXC Laboratory).

Approach/Strategy
(Beyond FY11)

After LTC experimentally demonstrates viability, launch joint development of full prototype LTC SiC growth system (fiber growth + lateral growth) in collaboration with commercial and/or university development partners.

Initiate basic GaN LTC experiments.

Projected Go/No Go:

- High growth rate of nearly defect-free boules
- Commercial investment to develop mass production of large wafers.
    - Several companies interested IF feasibility demonstrated.

Summary

Large Tapered Crystal (LTC) growth is a radically new (but experimentally unproven) game changing approach to SiC wafer growth offering the potential to drastically lower material defects and cost that are presently major inhibitors preventing wide adoption of SiC high-power devices that would enable large improvements to EV power converter size and efficiency.

This recently-initiated NASA/DoE study is starting to carry out experimental proof-of-concept of LTC growth with clear go/no-go for further investment/development.
- Two years to modify NASA hardware and demonstrate two never-before experimentally demonstrated “lateral” and “fiber” SiC growth processes.

If successful, fully developed LTC wafer production would enable far superior EV power electronics with significantly improved efficiency and size.