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New Metallization Technique Suitable for 6-MW Pilot Production of Efficient Multicrystalline Solar Cells Using Upgraded Metallurgical Silicon

Final Technical Progress Report
December 17, 2007 – June 16, 2009

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CaliSolar, Inc.
Sunnyvale, California

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Subcontract Report
NREL/SR-520-48591
August 2010

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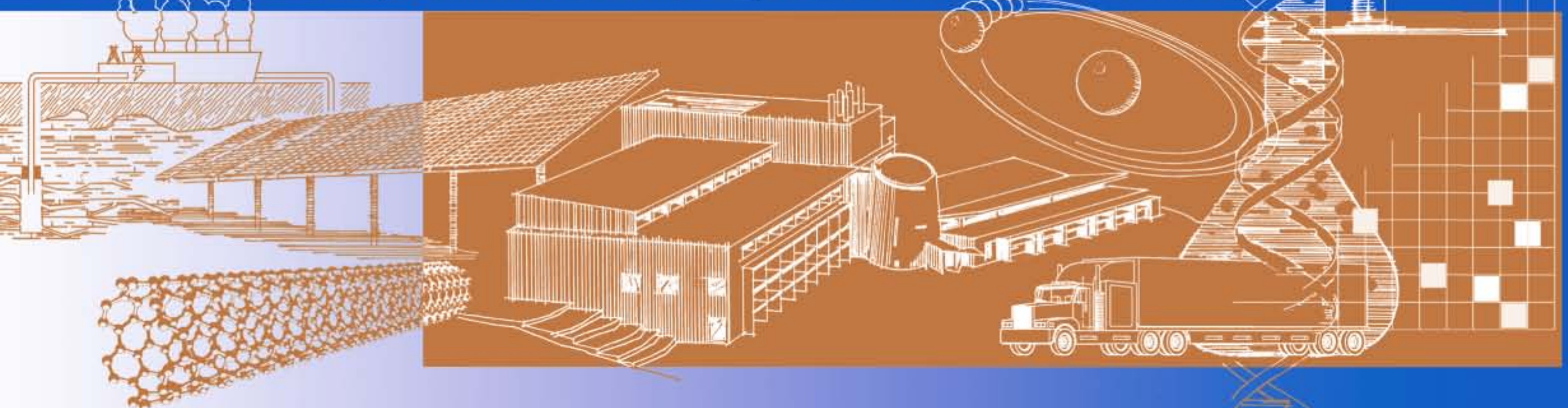

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NREL Technical Monitor: Richard L. Mitchell
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1. Summary

During the last 18 months, CaliSolar has enjoyed major success as a Photovoltaic Technology Incubator awardee within the U.S. Department of Energy's (DOE's) Solar Energy Technologies Program. Over this time span, the company evolved from a handful of employees to more than 100 scientists, engineers, technicians, and operators. On the technical side, the company transitioned itself from a proof-of-concept through pilot-scale to large-scale industrial production in just over two years. A fully automated 60-megawatt (MW) manufacturing line has been developed and commissioned in Sunnyvale, California. The facility is vertically integrated, converting upgraded metallurgical-grade (UMG) silicon (Si) feedstock to ingots, wafers, and high-efficiency, multicrystalline solar cells.

CaliSolar has pioneered the development and commercialization of high-efficiency Si solar cells based on 100% UMG Si feedstock. The technology we developed covers the whole value chain from Si feedstock to solar cells. We have developed an advanced casting process that results in UMG wafers with lifetimes exceeding 30 μs. Further, various parts of the cell were optimized to achieve conversion efficiencies competitive with those based on electronic-grade Si, but at significantly lower cost. During the period of this project, CaliSolar greatly improved its casting process, increased the size of its solar cells from 125 mm to 156 mm, optimized the front and back metal contacts, and improved the hydrogen passivation process. Collectively, these improvements have resulted in a champion cell efficiency of 16.73%, and the mean cell efficiency increased from 13.5% to 15.8% over a period of two years.

CaliSolar has partnered with major module manufacturers to test and qualify its cells. Modules of quality and reliability comparable to those based on electronic-grade Si cells were demonstrated. Additionally, various accelerated lifetime testing schemes showed little or no degradation in module efficiency.

2. Research and Development Activities

The tasks carried out to reach the ultimate objectives of the program included work on the development of laser grooving and electroplating for front contacts, optimization of the surface passivation and back contact, the optimization of impurity gettering and bulk passivation, and the development of a robust cell processing technology based on UMG Si. Much effort during Phase II was spent on the improvement of the cell and module efficiencies and the establishment of the manufacturing line.

2.1. Optimization of Laser-Grooved Front Contacts

The first phase of this contract was mainly concerned with technology optimization. We focused our development activity primarily on laser grooving for front-side contact and on the electroplating processes for the front-side metallization. We were also able to demonstrate the maturity of our novel technology by establishing a baseline of 14% cell efficiency on 100% UMG Si wafers early in this contract.

During the first quarter, we validated the process flow to form laser-grooved front contacts on 100% UMG Si multicrystalline wafers (125 mm x 125 mm). The laser used was a 1,064-nm Nd:YAG laser with a power of 100/20 W. During the experiments, different laser parameters such as speed, frequency, and current were varied to optimize the process and to create grooves with 30-µm width and 20-µm depth before KOH etching. A SEM cross section of a trench created by laser ablation is shown in Figure 1. We can clearly observe a lot of residues on the side of the trench either on top of the antireflection coating (ARC) layer on the flat surface of the wafer, or within the trench.

These residues were subsequently removed in a KOH bath. Approximately 5 µm of the damaged Si region in the trench and all the residues on the top of the ARC were removed. A clean trench and the top ARC surface are shown in Figure 2. The optimization of the laser ablation process allowed us to develop contact trenches with 50 µm width after damage removal, hence meeting the requirements of the deliverable.

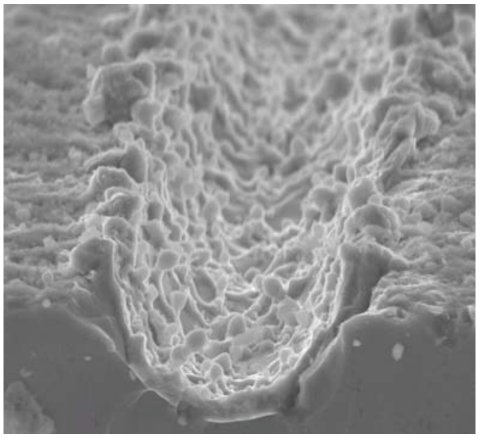


Figure 1. SEM image of a laser-grooved wafer

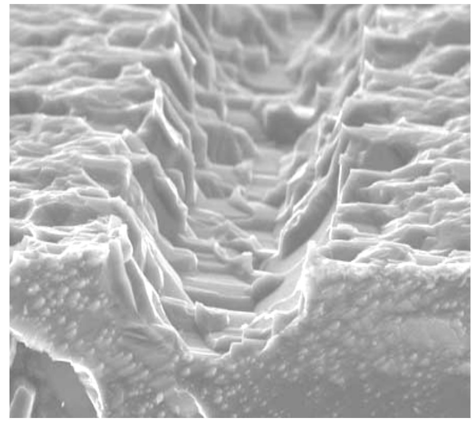


Figure 2. SEM image of laser-grooved wafer after damage removal

The above deliverable was an intermediate milestone for our development work to demonstrate trenches with a width of <30 μm. The laser used for the latter was a UV laser at 354-nm wavelength. During the experiments, the laser parameters such as speed, frequency, and current were varied to optimize the process. The ultimate goal of this trial was to get trench width < 20 μm after laser etching, while keeping the width less than 30 μm after laser damage removal (Figure 3). The main difficulty was to keep the width of the trench independent of the grain orientation in our polycrystalline wafers.

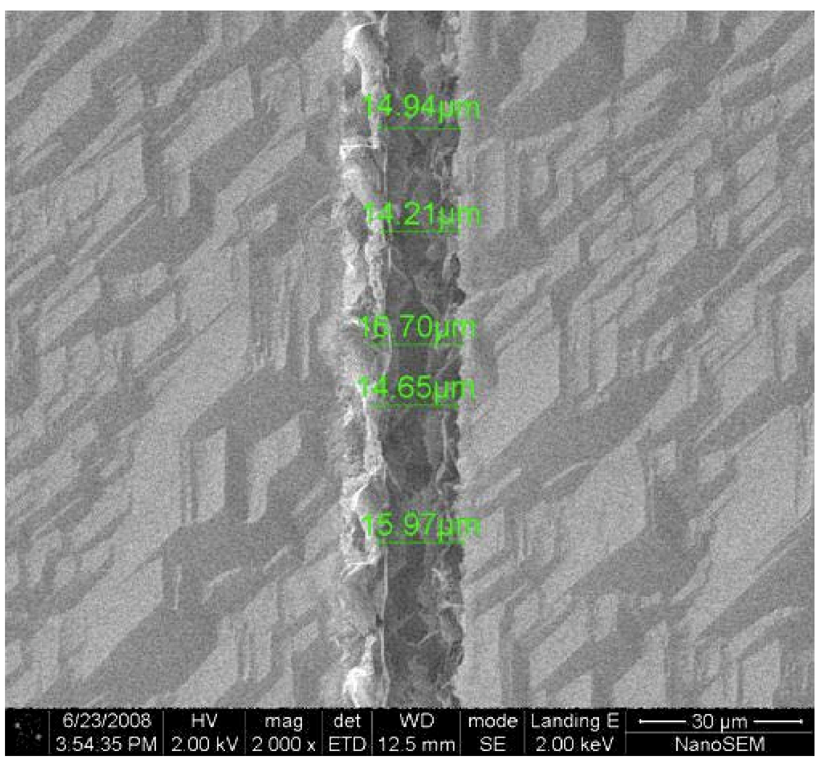


Figure 3. SEM plan view of a <20-μm-wide trench after laser damage removal

2.2. Electroplating Development

The goal of this task is to develop a metal deposition process using metal-plating techniques instead of the conventional screen-printing metallization. The main advantage of this technique is to form metallic lines at low temperatures with a high aspect ratio, good contact to the emitter, and low electrical resistance. The process temperature required is less than 500°C in order to retain the benefits of the gettering of the metallic impurities in the bulk UMG Si. The first step of the development was to demonstrate a metal-plating process capable of filling a 70-µm-wide trench with a first electrolessly deposited metal layer with low contact resistance to n+ type Si and good barrier properties to Cu. The latter is subsequently deposited with an electroplating process. This metal-plating process was demonstrated on laser-grooved front side contacts with an n+/n++ emitter with a resistivity of 100 and 10 Ω/□, respectively (Figure 4).

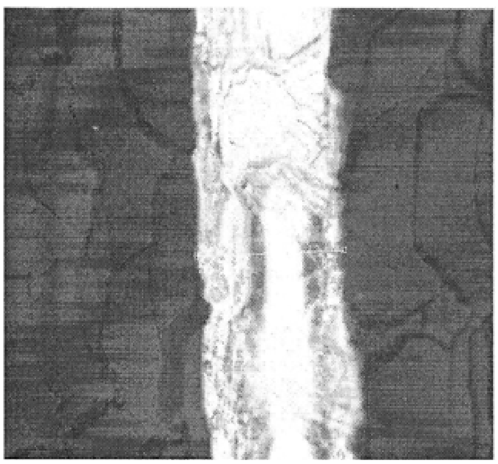


Figure 4a. Plan view of a 56-µm-wide laser-grooved trench filled with electroplated copper

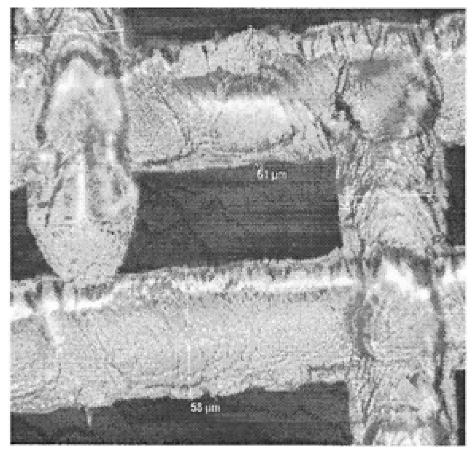


Figure 4b. Plan view of an interdigitated bus bar on the same wafer in Figure 4a

Our initial efforts were to develop the capability of filling 70-µm-wide trenches, first with an electrolessly deposited metal layer with low contact resistance to n+ type Si and good barrier properties to copper, which is subsequently deposited with an electroplating process. After the optimization of the groove cleaning, prior to metal plating and the process conditions for metal plating, we demonstrated a continuous filling of ~30-µm-wide trenches with electroplated metal (Fig. 5). This metal plating process resulted in laser-grooved front-side contacts with an n+/n++ emitter with a resistivity of 100 and 10 Ω/□, respectively.

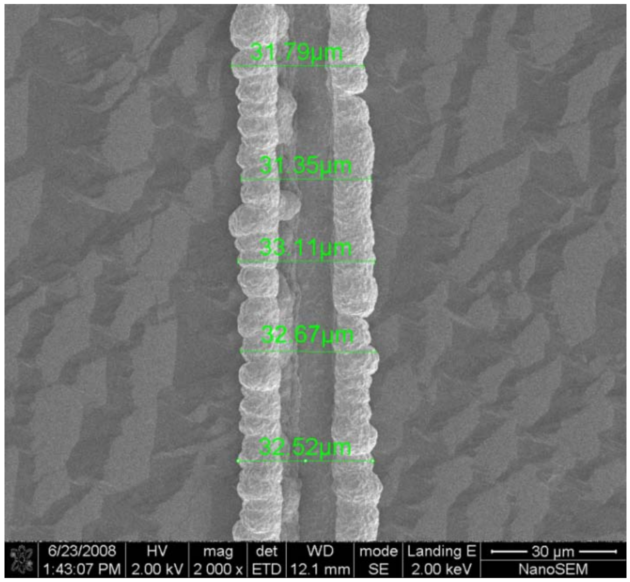


Figure 5. SEM plan view of <50-µm-wide trenches in Si filled with an electroless metal-plating deposited film

In the second phase of this project, we carried out the metallization development activities with some changes that were introduced to make the process more compatible with large-scale industrial production. This decision was driven by a careful study of the cost of producing the cells with this new metallization, and by risk mitigation to ramp up the factory using a well-stabilized process on a manufacturing proven tool. With this new approach, the new metallization procedure was based on front-side screen printing with optimized printing of narrower fingers. After co-firing and before laser edge isolation, the plating process takes place. Subsequently, the plating, the edge isolation, and the sorting are carried out. The goal is to improve the front contact by electrodepositing dense layers on printed fingers. Therefore, the improvement in cell performance is due to better series resistance.

The plating is an electrochemical, potential bias-enhanced deposition process. First a Ni layer is plated on the screen-printed Ag fingers. The Ni layer is only 1.5 µm thick and the goal is to prevent the Cu from diffusing into the Si. After rinsing the wafer, the Cu layer is deposited on the Ni. The thickness of the Cu layer determines the conductivity of the fingers. In this work, ~ 8-µm-thick layers were deposited. In the last step, performed after rising, a 3-µm-thick Sn layer is deposited. The Sn layer is needed for the soldering of the cells. An SEM cross section of a plated finger is shown in Figure 6.

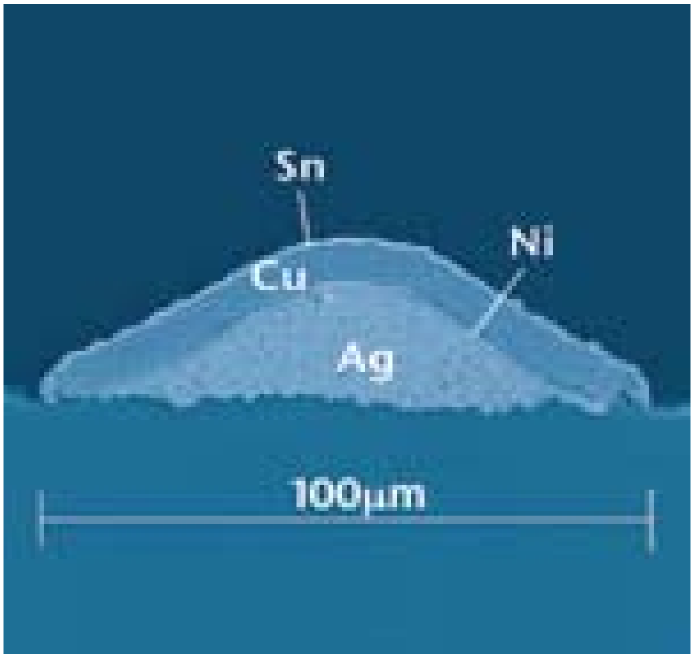
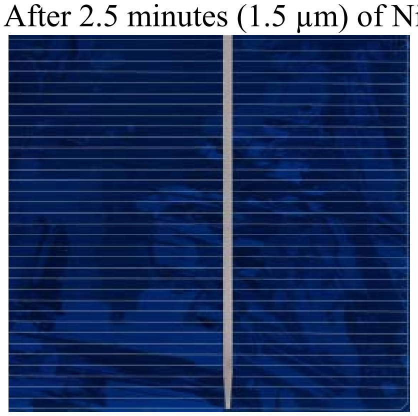
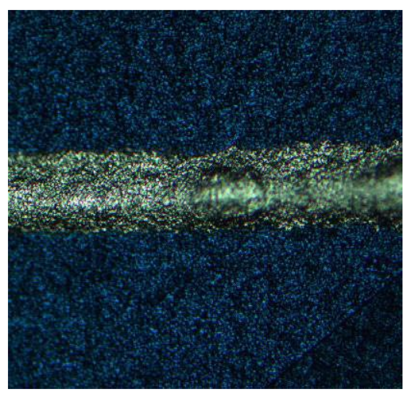


Figure 6. SEM cross section of copper electroplated on a screen-printed finger

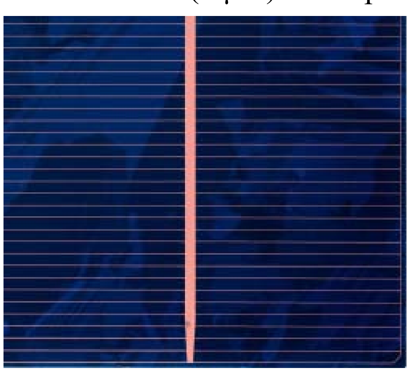
The plating process is sequentially illustrated in Figure 7 below.

After 2.5 minutes (1.5 µm) of Ni plating





After 6 minutes (8 µm) of Cu plating



After 2 minutes (3 μm) of Sn plating

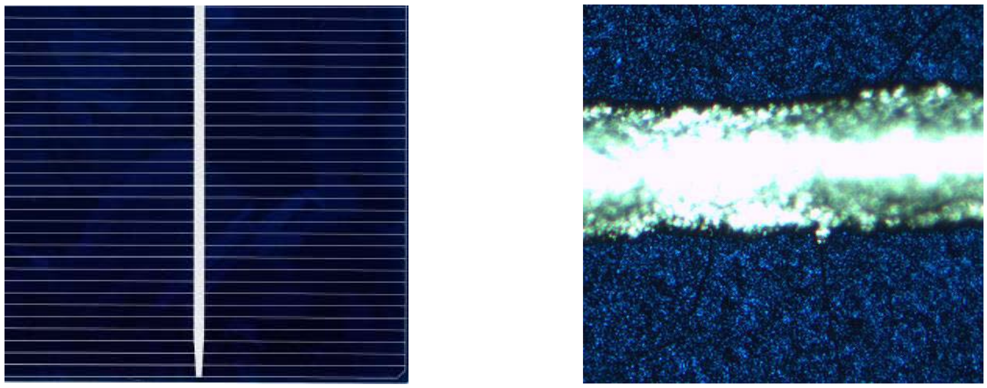


Figure 7. Optical micrographs illustrating the electroplating sequence

2.3. Surface Passivation

As in conventional Si solar cell technology, good surface passivation is a critical step for achieving good cell performance in UMG-based cells. Our process consists of hydrogenation of Si with microwave induced remote hydrogen plasma (MIRHP). The conditions for optimal hydrogenation were studied in relation to the sample conditions, such as the surface texturing and the active carrier concentration in the bulk. This hydrogenation process is key to obtaining good efficiency when using a low thermal budget with electroplated metallization.

2.4. Solar Cells

Obtaining cell efficiencies on 100% UMG cells that are comparable to those obtained from electronic-grade cells, but with a significant cost advantage, was a key aspect of this work. At the beginning of this project our mean efficiency was around 13.5%. One of the most important milestones in this project was reaching cell efficiencies of 16% based on 100% UMG Si. This was reached in December 2008 with the demonstration of energy conversion efficiency greater than 16% on two 6-in. cells using 100% UMG Si feedstock. The conversion efficiency measured was 16.24% and 16.23%, respectively. These values were confirmed by NREL's Cell Measurement Group. The process used to demonstrate these high efficiencies was basically the same as our baseline process, but with several process improvements enabling this major enhancement in cell efficiency. The main contributors were:

i. Optimization of the groove etching and cleaning process, enabling a more uniform growth of the electroplated film
ii. Improvement of the passivation of bulk defects by better control of the release of hydrogen from the ARC layers and during the last hydrogenation step
iii. Optimization of the Si casting process.

On January 9, 2009, eight additional cells with the electrical characteristics reported in Table 1 below were sent to NREL for the main cell efficiency deliverable (deliverable D-14).

Table 1. Electrical Characteristics of the Cells Sent to NREL for Deliverable D-14

Nr	Cell-ID	Area	Temp	FF	jsc	Voc	Eta
1	H102C_098	151.29	25.1	77.95	33.04	625.8	16.11
2	H102C_066	151.29	25	78.22	32.74	627.5	16.07
3	H102C_063	151.29	25	78.54	32.62	627.2	16.07
4	H102C_080	151.29	25.1	78.32	32.61	628.2	16.05
5	H102C_092	151.29	25	77.92	32.84	626.2	16.03
6	H102C_086	151.29	25	78.09	32.74	627.3	16.04
7	H102C_076	151.29	25	78.45	32.53	628	16.03
8	H102C_056	151.29	25	78.35	32.59	626.8	16.01
9	H102A_054	141.61	25	79.74	32.44	627.6	16.24
10	H102A_055	141.61	25	79.59	32.5	627.6	16.23

2.5. Mini-Modules

One of the peculiarities of solar cells built with 100% UMG Si is that they exhibit a significantly lower diode-breakdown voltage compared to cells processed with electronic-grade Si. This parameter is important in case some cells are shaded on a fully operational module. In a worst-case scenario, where just one cell is shaded whereas all other cells in the string are under full illumination, the shaded cell functions as a load that resists the total voltage of the string and the voltage of the bypass diode. One solution could be to reduce the length of the string, but at a higher cost for the module manufacturer. A very elegant alternative solution was proposed by Day4Energy, whose module concept will not be disclosed in this report due to confidentiality issues.

We decided to use Day4Energy for building the modules to be delivered to NREL. One of the main advantages of this assembly technique is that no busbar is required for the front side, hence reducing the light shadowing. The cells' characteristics used for this deliverable are reported in Table 2. Compared to the cells of Table 1, processed with a front side with a busbar, we can observe, as expected, a significant increase in both the short-circuit current and the energy conversion efficiency with several cells at a 16.4% efficiency record for CaliSolar. The cells were sorted by I_{mpp}; the 12 best cells were assembled into two 6-cell mini-modules.

Table 2. Cells Used in the Fabrication of Mini-Modules

	(V)	(A)	(mA/cm²)	(W)	(V)	(A)	(%)	(%)
Serial Number	Voc	Isc	Jsc	Pmpp	Vmpp	Impp	FF	η
H1026-2-114	0.628	5.065	33.482	2.476	0.519	4.766	77.8	16.4
H1026-3-110	0.627	5.045	33.345	2.446	0.515	4.748	77.3	16.2
H1026-1-117	0.627	5.056	33.421	2.482	0.523	4.746	78.3	16.4
H1026-3-107	0.628	5.052	33.394	2.472	0.522	4.735	77.9	16.3
H1026-2-119	0.626	5.051	33.383	2.484	0.525	4.735	78.5	16.4
H1026-1-124	0.627	5.053	33.401	2.476	0.523	4.732	78.1	16.4
H1026-1-120	0.627	5.048	33.369	2.486	0.526	4.730	78.5	16.4
H1026-2-044	0.627	5.036	33.285	2.480	0.525	4.728	78.5	16.4
H1026-2-112	0.627	5.048	33.365	2.488	0.528	4.712	78.6	16.4
H1026-1-125	0.626	5.057	33.426	2.470	0.525	4.708	78.0	16.3
H1026-1-103	0.627	5.047	33.359	2.459	0.522	4.707	77.7	16.3
H1026-2-039	0.626	5.013	33.132	2.471	0.525	4.705	78.7	16.3
H1026-2-133	0.626	5.038	33.299	2.469	0.525	4.702	78.3	16.3
H1026-4-040	0.625	5.003	33.071	2.463	0.524	4.701	78.7	16.3
H1026-3-037	0.625	4.992	32.995	2.452	0.522	4.698	78.6	16.2
H1026-3-038	0.625	4.998	33.037	2.453	0.522	4.696	78.5	16.2
H1026-1-132	0.624	5.020	33.179	2.441	0.520	4.691	77.9	16.1
H1026-3-118	0.627	5.043	33.336	2.472	0.528	4.683	78.2	16.3
H1026-3-126	0.623	5.004	33.074	2.443	0.522	4.676	78.3	16.1
H1026-4-034	0.625	4.975	32.885	2.446	0.524	4.670	78.7	16.2
H1026-4-030	0.625	4.978	32.904	2.458	0.526	4.668	79.0	16.2
H1026-4-032	0.625	4.971	32.857	2.449	0.525	4.665	78.9	16.2
H1026-4-031	0.625	4.966	32.822	2.444	0.524	4.661	78.8	16.2
H1026-4-033	0.626	4.989	32.979	2.455	0.528	4.653	78.7	16.2

2.6. Commercial-Size Modules and Module Reliability

Beginning in April 2008, CaliSolar started to make contact with different major module manufacturers interested in evaluating solar cells based on UMG Si. Our selection was based on the capability of the engineering department of the company we partnered with to support our request, in case some problem would appear because of the specificity of our material.

To make our cells more compatible with mainstream module manufacturers, considerable efforts were put into investigating the main causes of lower breakdown voltage in UMG-based cells. Steady improvement in the quality of our feedstock and the casting conditions have yielded breakdown voltages >12 V, as evidenced in Figure 8.

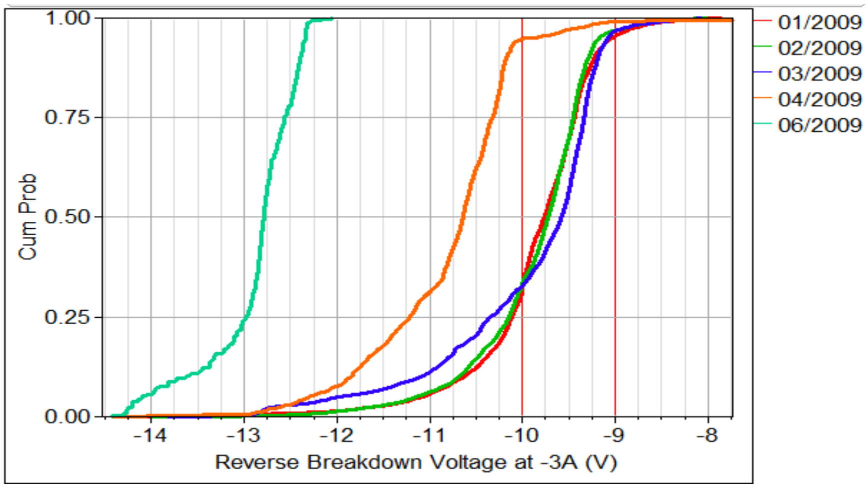


Figure 8. Steady improvement in our UMG technology has yielded breakdown voltages >12 V.

Particular emphasis was placed on cell and module reliability. One important degradation mechanism that we investigated was light-induced degradation (LID). With a non-optimized UMG cell process, a marked degradation in short-circuit current and efficiency was observed (Figure 9). However, with the improvement of the quality of our UMG feedstocks and the casting conditions, CaliSolar's UMG and electronic-grade Si devices can have equally low LID.

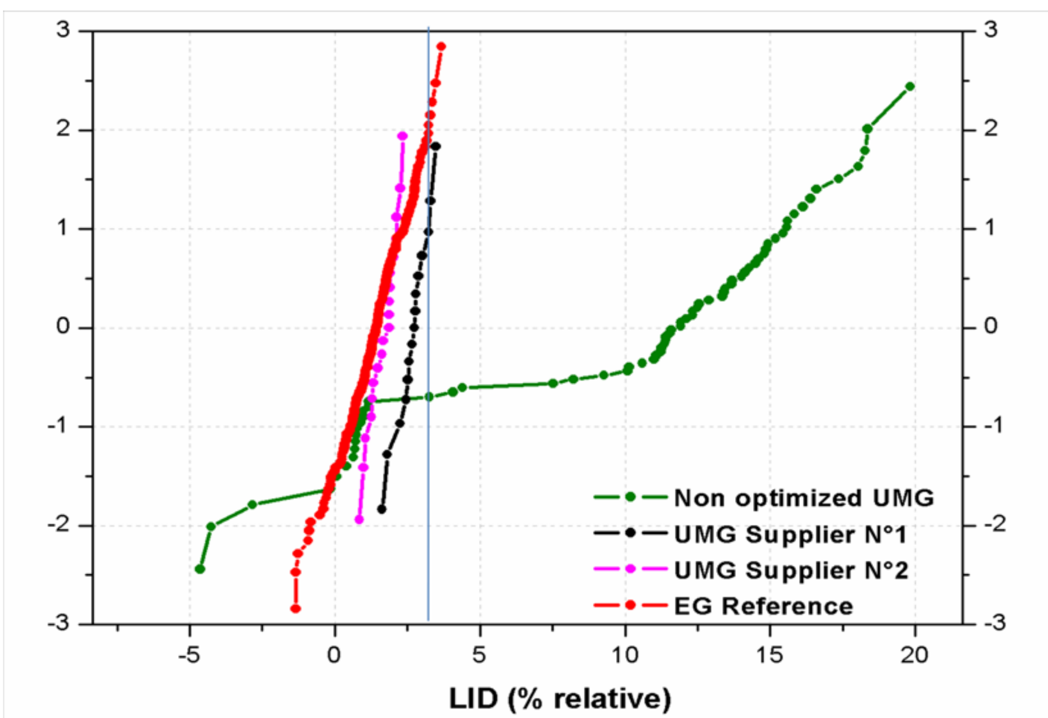


Figure 9. CaliSolar UMG and electronic-grade Si can have equally low light-induced degradation.

2.7. Pilot Production

In keeping with the PV Technology Incubator concept of starting with a prototype and ending with a pilot line, we invested considerable resources in setting up a 6-MW pilot line in Sunnyvale, California. This was accomplished by the end of Phase I of this project. Operating this pilot line proved to be critical in testing and further improving various steps in our fabrication process. Further, it was a necessary prerequisite to setting up our manufacturing line. The experience we gained in pilot operation proved invaluable in tool selection for the production line and also in the development of our cell efficiencies.

Cell efficiency improvement has been a main focus area throughout this project. Figure 10 shows the evolution of cell efficiency with time from the beginning of this project to date. Clearly, the optimization of the casting conditions and various cell parameters has resulted in a dramatic increase in cell efficiency. Currently, our champion cell has an efficiency of 16.73%. Some of these improvements were integral parts of this PV Incubator project. However, many other process developments were not directly related to this project, but nonetheless were well-aligned with the DOE Solar Program's goals of reducing the cost of solar electricity.

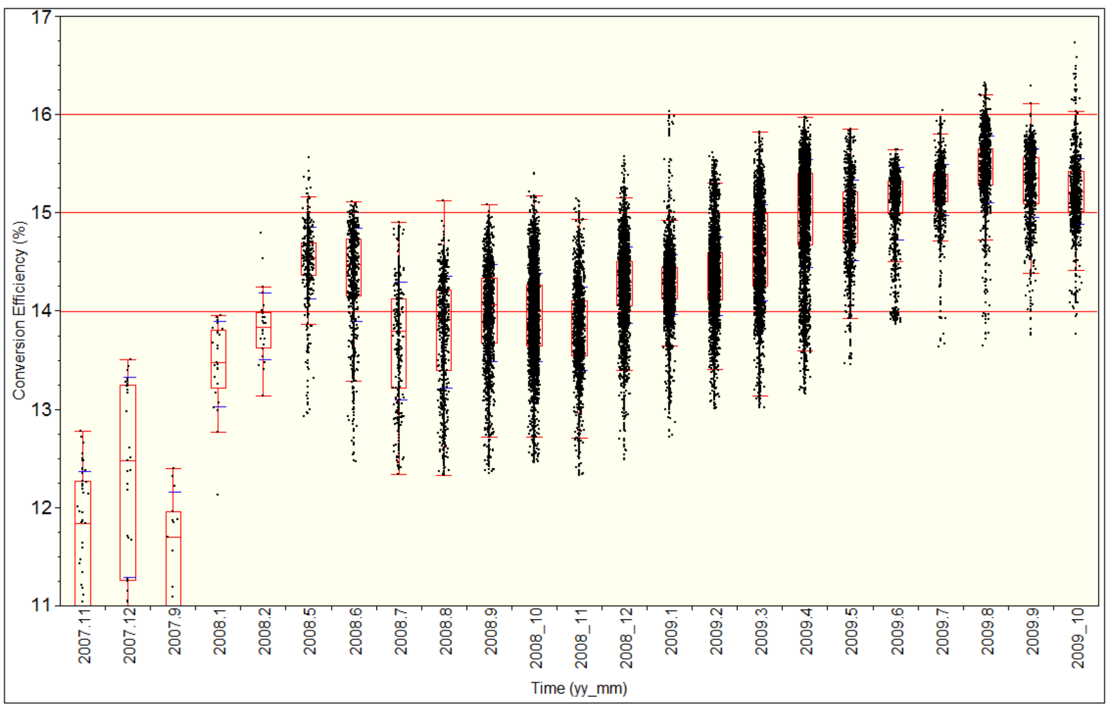


Figure 10. Cell efficiency evolution within the duration of this project

2.8. Building a 60-MW Manufacturing Line and Future Projections

CaliSolar was able to close the second round of funding to build a 60-MW commercial plant. Different locations were investigated worldwide. This selection process was quickly narrowed down to California and more precisely to the south of the Bay Area. Among more than 10 potential industrial sites, a 130,000-ft^2 site in Sunnyvale was selected at the end of October 2008, and the lease was signed on December 17th. The design of the production floor layout started as soon as the site was selected. All facilities work was defined and the demolition work started on December 18.

The tool selection process started as early as June of 2008. The methodology used for the tool selection was as scientific as it could be to identify the best equipment available on the market that was compatible with our technology. Purchase orders were issued between August and November for various pieces of equipment, such as casting furnaces, wet-benches, diffusion furnaces, and devices for antireflective coating and metallization. The most critical point during the negotiation with the vendors was the delivery time, as the backlog of orders for all vendors was varying between 18 weeks and 16 months! The strong interest of the PV community in UMG Si helped CaliSolar draw the attention of the tool suppliers and shorten the delivery time.

In addition to tool selection and purchasing, massive site preparation, and equipment installation, CaliSolar experienced a rapid increase in staffing. Currently, it employs nearly 100 engineers and technicians. At the time of writing this report, both production lines are up and running with various test runs being completed. It is expected that within three months the plant will be running at full one-shift capacity (Figure 11).

Figure 11. CaliSolar's 130,000-ft^2 site housing the 60-MW plant. Photo credit: CaliSolar

3. Conclusions

Most of the goals of this PV Incubator project were reached. CaliSolar was successful in transferring its novel UMG Si-based cell technology from the concept and feasibility phase, through a batch-pilot phase, and into large-scale manufacturing. The company drove technology in three areas: crystallization, wafer treatment, and cell processing. The cell size was increased from 125 mm to the industry standard of 156 mm, while the mean cell efficiency increased from 13.5% at the beginning of this project to 15.8% in pilot production in 2009 with peak efficiency at 16.73%. The company transitioned from a handful of employees in 2007 to nearly 100 engineers and technicians at the present time.

At the time of writing this report, the company is operating a 60-MW, full manufacturing line complete with ingot casting, wafering, and advanced cell processing in a 130,000-ft^2 facility in Sunnyvale, California.

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14. ABSTRACT *(Maximum 200 Words)*
This report describes CaliSolar's work as a Photovoltaic Technology Incubator awardee within the U.S. Department of Energy's Solar Energy Technologies Program. The term of this subcontract with the National Renewable Energy Laboratory was two years. During this time, CaliSolar evolved from a handful of employees to over 100 scientists, engineers, technicians, and operators. On the technical side, the company transitioned from a proof-of-concept through pilot-scale to large-scale industrial production. A fully automated 60-megawatt manufacturing line was commissioned in Sunnyvale, California. The facility converts upgraded metallurgical-grade silicon feedstock to ingots, wafers, and high-efficiency multicrystalline solar cells.

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