High Temperature DC-Bus Capacitor Cost Reduction and Performance Improvements

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Sigma Technologies International

6/7/2016

Project ID #: **EDT059**

Overview

Timeline

- Start date – October 1, 2013
- End date – July 30, 2016
- Percent complete – 75% as of 3/31/2016

Budget

- Total funding: $3,510,987
  - DOE share: $2,288,599
  - Contractor share: $1,222,338
- Expenditure of funds in
  - FY13: $129,484
  - FY14: $1,239,821
  - FY15: $996,153
  - FY16: $204,622 (3/31/16)
  - Total: $2,570,080

Barriers addressed

- A & C (Cost & Weight): Overall size and cost of inverters, as well as thermal management system
- D (Performance and Lifetime): High-temperature operation
  - The performance and lifetime of capacitors available today degrade rapidly with increasing temperature (ripple current capability decreases with temperature increase from 85˚C to 105˚C)

Partners

- Interactions / collaborations
  - Delphi Automotive Systems
  - Oak Ridge National Laboratory
  - Project lead: Sigma Technologies

Relevance/Objectives

- Overall Objectives
  - Reduce the cost, size and weight of the DC-link capacitor by >50%
  - Increase durability in high temperature environments
- Objectives this period
  - Define size and shape of PML capacitor
  - Develop thermal-mechanical and electrical models of the Gen1 capacitor
  - Complete upgrade pilot line
  - Finalize PML dielectric
- Impact
  - Accelerate the manufacturing capability and mass production adoption of energy-efficient and cost-effective APEEM capacitor technologies into electric drive vehicles, such as electric vehicles (EVs), hybrid electric vehicles (HEVs), and plug-in hybrid electric vehicles (PHEVs)

Project Milestones

Month/ Year	Milestone or Go /No-Go Decision	Description	Status
June 2015	Milestone	Completion of the upgrades for the Gen1 prototype capacitor pilot line	Completed
June 2015	Go/No-Go Decision	Gen1 prototype capacitor testing and evaluation of capacitor performance and the potential of the dielectric material and capacitors to meet or exceed the capacitor targets	Completed

Approach – Overcome Limitations of Polypropylene (PP) DC-Link Capacitors

- Current baseline PP DC-link capacitors are large (~1 liter), heavy (~1 kg), temperature limited (105˚C) and costly
- Metallized PP capacitors must be derated from 85˚C to 105˚C by at least 30%, which is >50% drop in energy density
- <u>PP DC-link capacitor supply chain:</u> Today's PP DC-link capacitors utilize extruded and biaxially oriented film produced and metallized by just a handful of film OEMs worldwide, as a result most capacitor OEMs produce similar products and there is limited opportunity for innovation

- Sigma has developed a solid state Polymer-Multi-Layer (PML) Having a prismatic shape with
- low ESL and ESR
- Operating temperature (T_{op}) range of -40°C < T_{op} < 140°C
- Dielectric constants in the range of 3.0 < k < 6.2 , Dissipation factor DF < 0.01
- High breakdown strength dielectrics
- Benign failure mode
- <u>Transformational and potentially disruptive technology</u>: Liquid monomer and Al wire are converted in a single step into Mother Capacitor material

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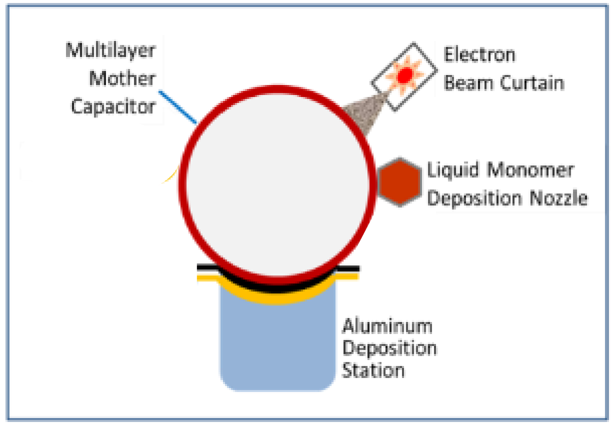
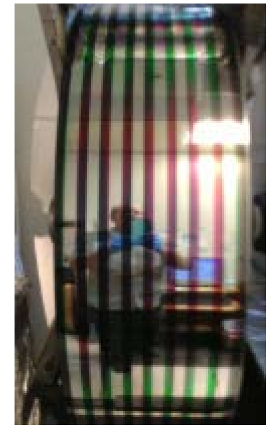
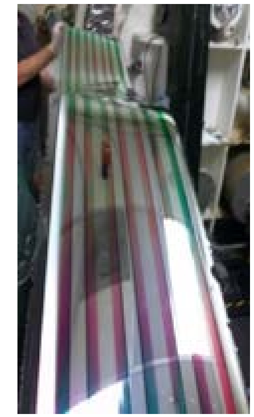
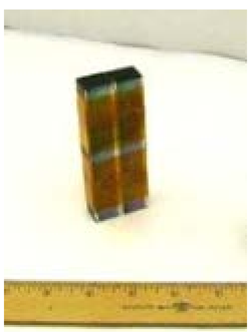
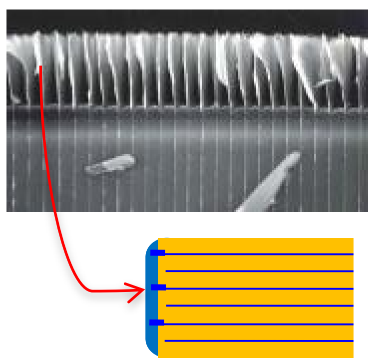
Approach – High Temperature, High energy density Polymer Multi-Layer (PML) DC-Link Capacitors











All aspects of capacitor manufacturing are controlled by the capacitor OEM

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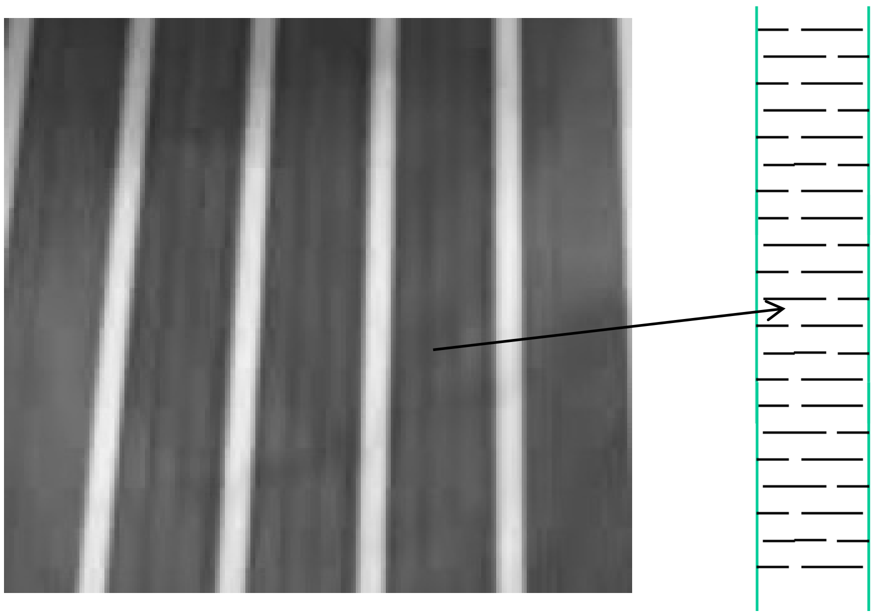
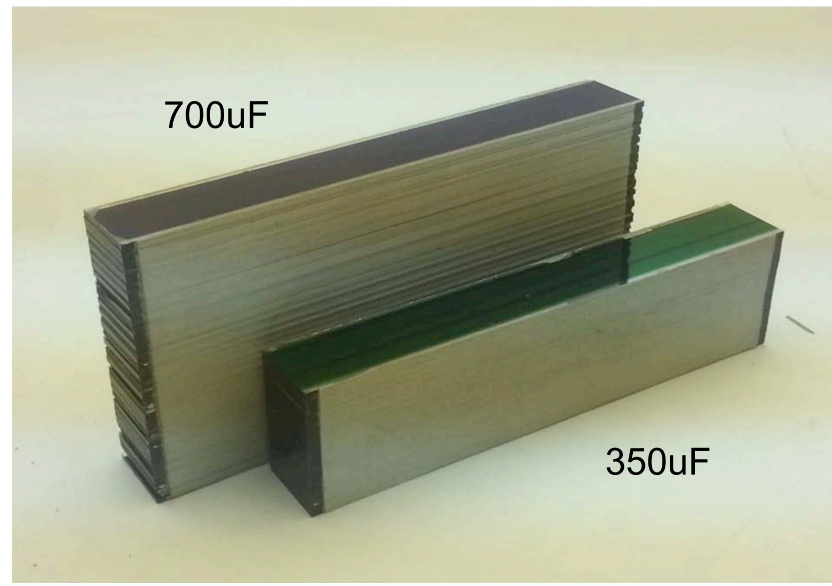
Develop a New Electrode Mask Which Double the Number of Capacitors Produced In a Single Run

Developed Internal Series Capacitors Which Reduce Volume Eliminate External Connections and Reduced ESR

Example: 700μF / 720Vmax PML capacitor with ESR<0.5 mohm





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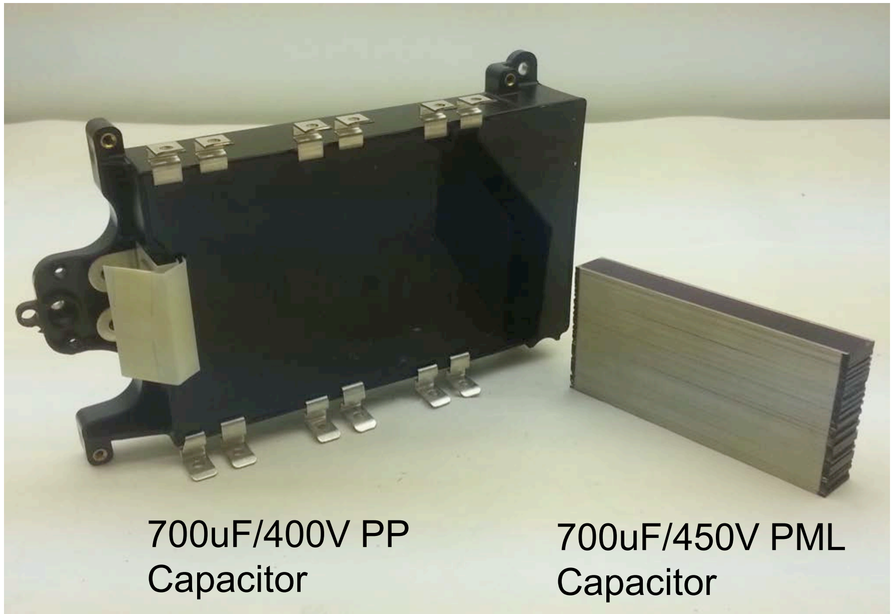
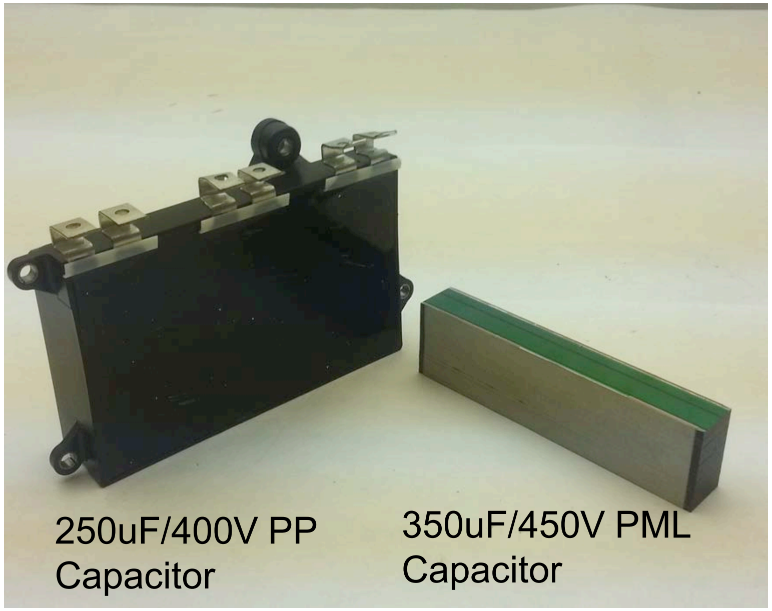
Dramatic Improvement in Volumetric Efficiency Over Conventional State of the Art Polypropylene Capacitors





350uF

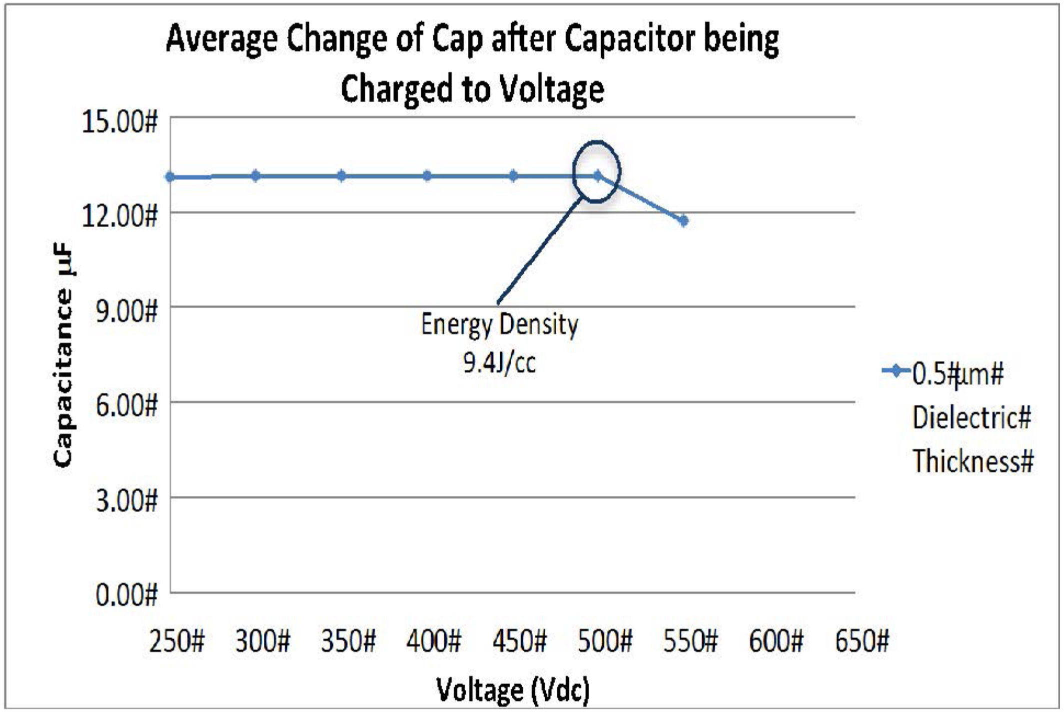
Record Energy Density

Capacitance variation with voltage of 1000 layer PML capacitor

0.5mm dielectric thickness.

At 500VDC the 0.5mm dielectric capacitors are stressed at 1000V/mm,

Higher not only than all other polymer dielectric capacitors, but even higher than the intrinsic breakdown strength of polymer film dielectrics (which is in the range of 400V/mm to 700V/mm)

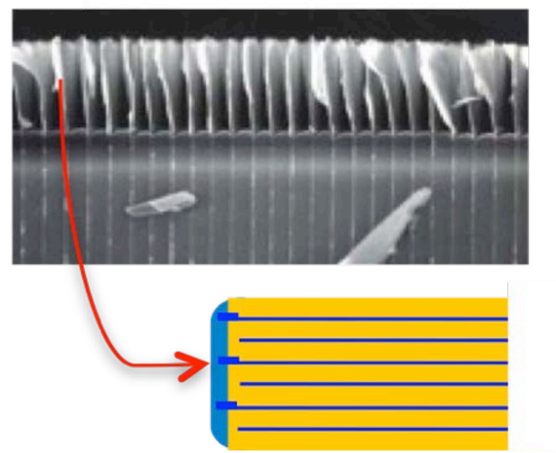


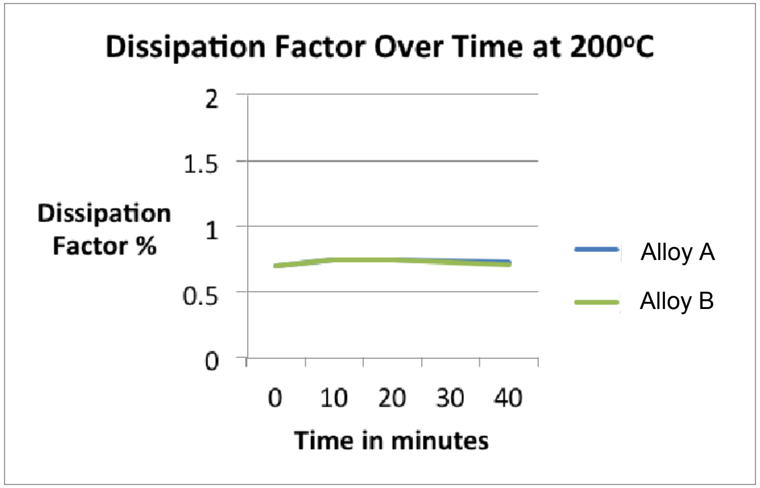
Optimization of Arc Spray Process (Electrode Termination)

A series of experiments were conducted to determine the best material for connecting-shorting the electrodes using an arc spray process

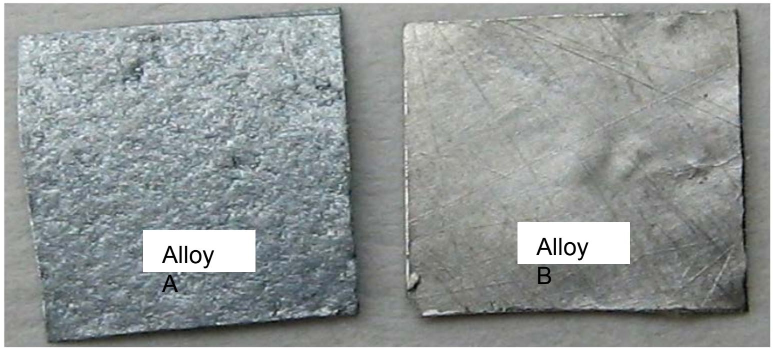
Zinc, Babbitt and various alloys are used to terminate metallized capacitors

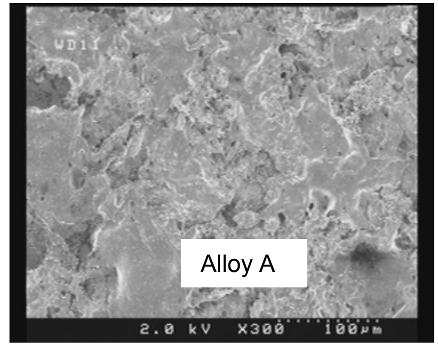
Several arc spray metals were tested and the selection was based mostly on the microstructure and corrosion properties

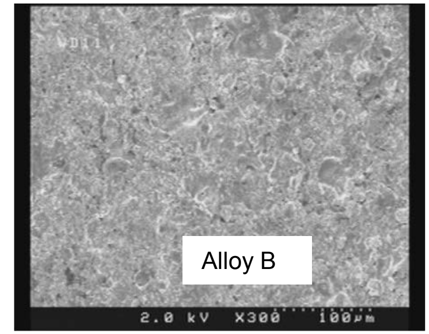




Optimization of Arc Spray Process (Electrode Termination)

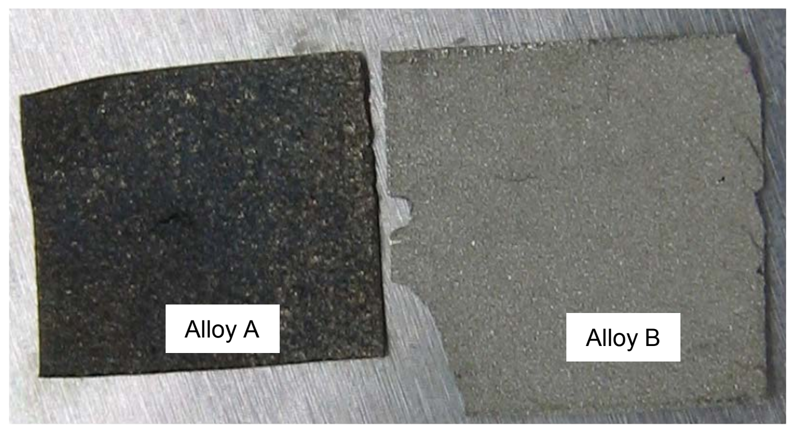






Alloy A has significantly coarser particle size that Alloy B

Alloy B was chosen based on the finer microstructure and corrosion resistance



After exposure to High Pressure Steam for 4 hrs

Passivation of the Aluminum Electrodes to Minimize Corrosion Degradation

Metallized capacitors can lose capacitance as a function of time when exposed to high temperature and humidity with bias, due to electrode corrosion

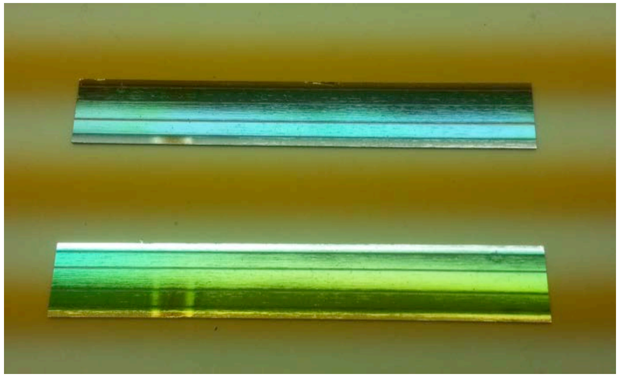
Thin aluminum electrodes (typically <20nm thick) will corrode if the capacitor is not adequately packaged

The aluminum electrodes in PML capacitors have superior corrosion resistance, via passivation:

a) inline with the aluminum deposition
b) a unique process has been developed that blocks moisture from reaching the aluminum by reacting the aluminum with an organic moiety,

Accelerated Corrosion Test
4hr Exposure to High Pressure Steam

PML Capacitor Before Test
Electrode Resistance > 10 ohm/sq

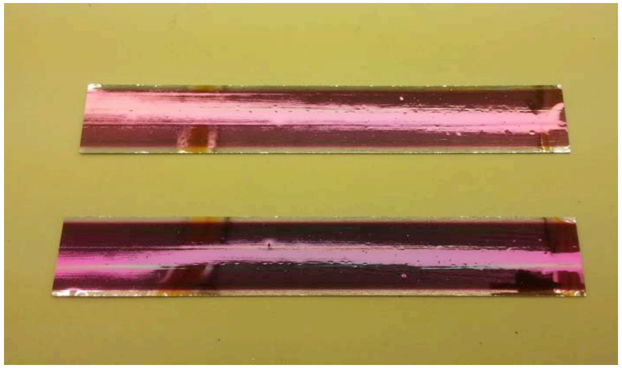


Metallized PP Capacitors Before Test
Electrode Resistance

3 ohm/sq

>10 ohm/sq

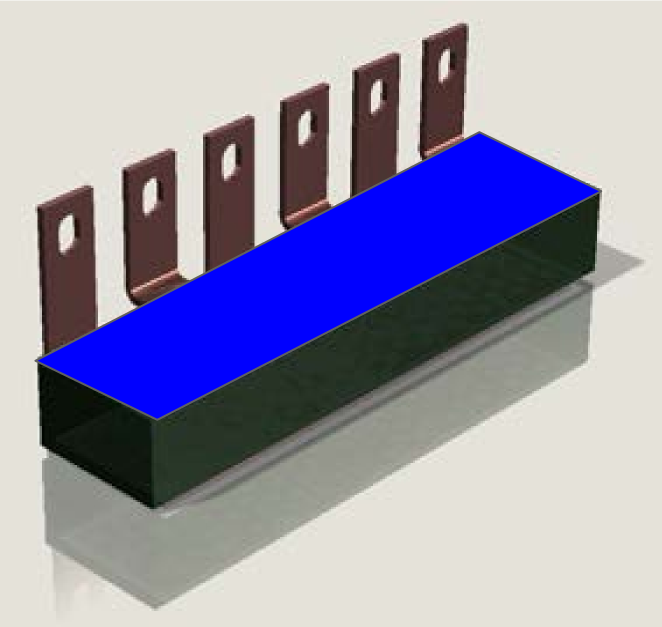
PML Capacitor After Test



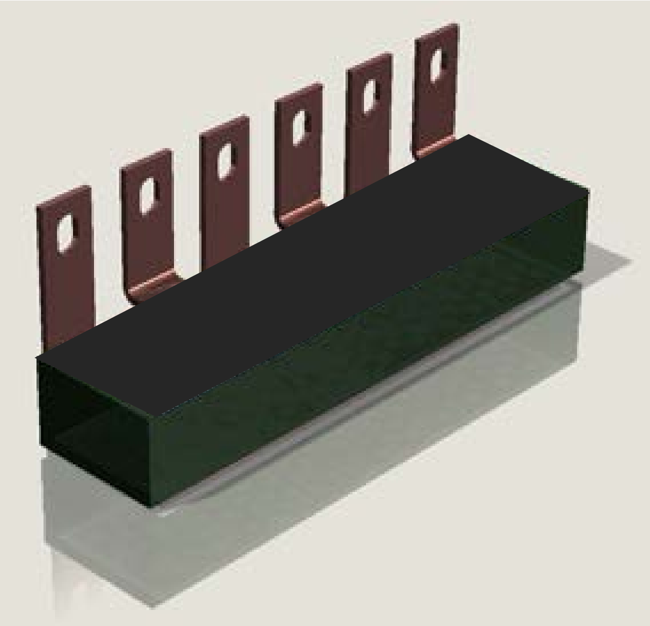
Metallized PP Capacitor After Test

Ongoing Work on Packaging Design

Potted in A Thermoplastic Box
Epoxy/Polyurethane Filled



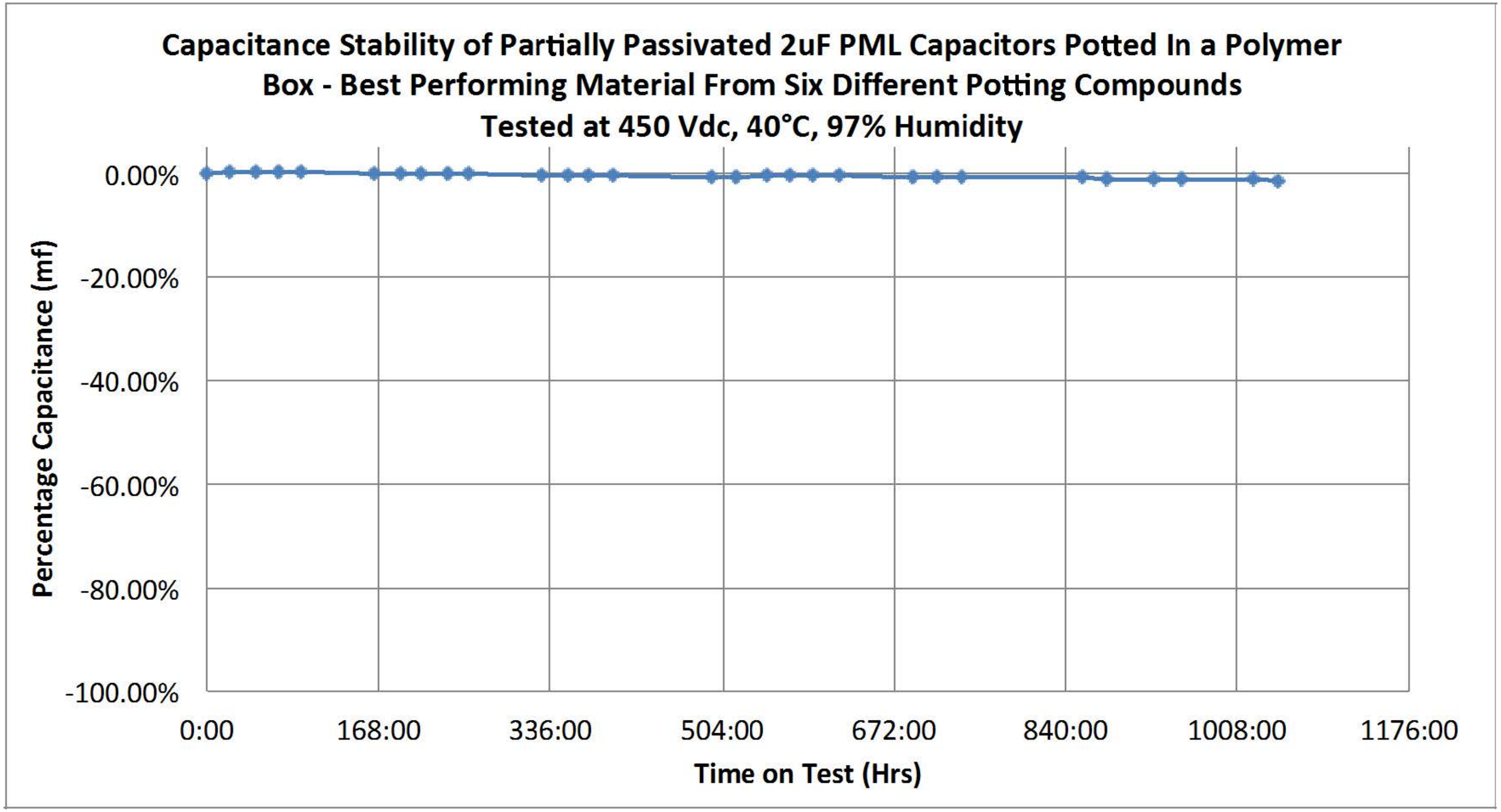
Transfer Molded Package



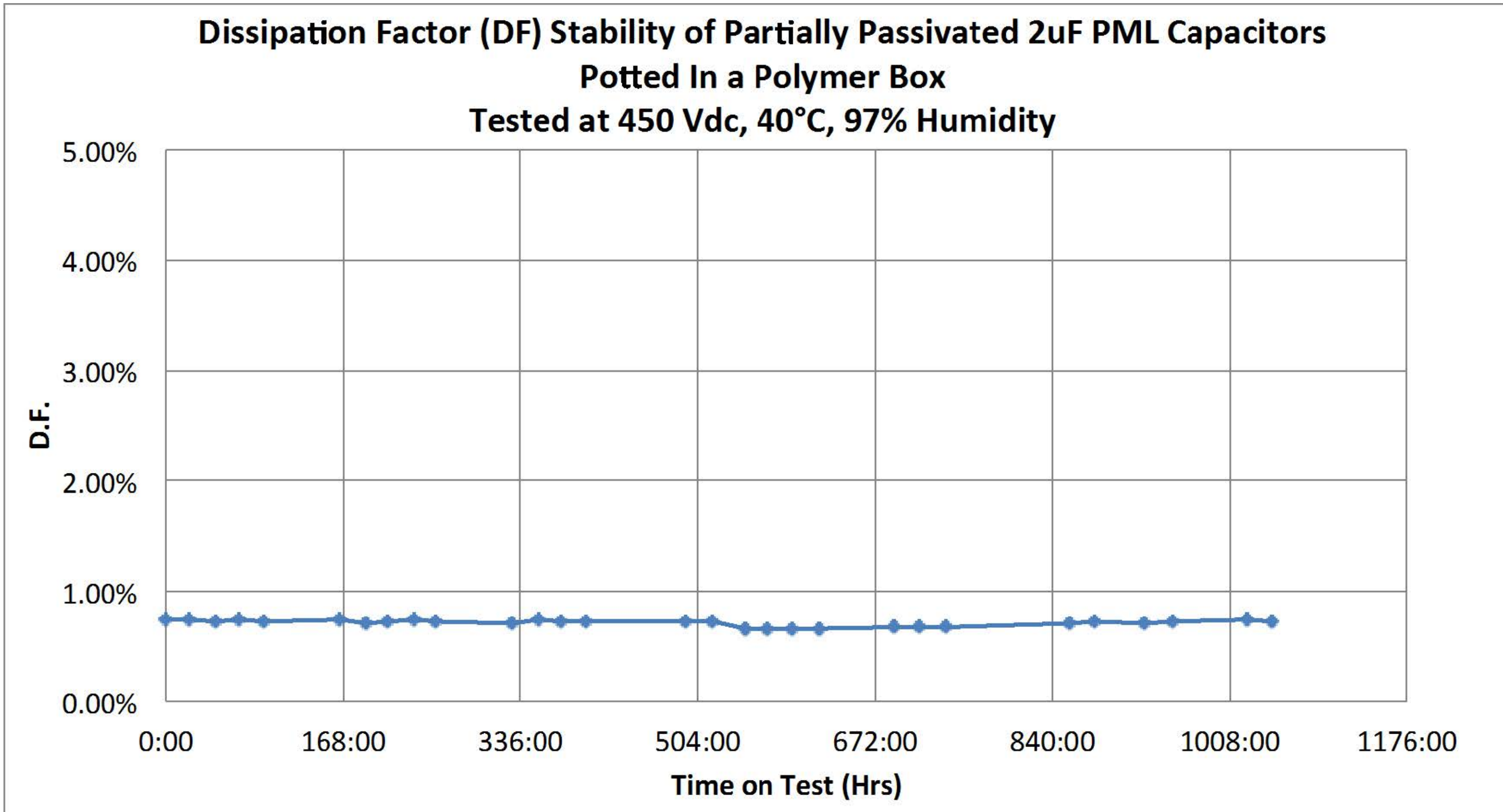
Capacitor Specifications and Testing

- Delphi has provided a capacitor specification that defines end-of-life requirements for capacitance, capacitance change over temperature, ESR, ESL, ripple currents, voltage ranges and isolation resistance
  - Includes information on how the parts are to be tested
  - Temperature range for testing is -40° C to 140° C
- Delphi has also provided life test requirements for the capacitor, including high temperature exposure, thermal cycling, bias humidity, physical and electrical characterizations, and flammability requirements

Preliminary Life Test Using a Potting Packaging Process Capacitance Stability as a Function of Time



Preliminary Life Test Using a Potting Packaging Process
Dissipation Factor Stability as a Function of Time



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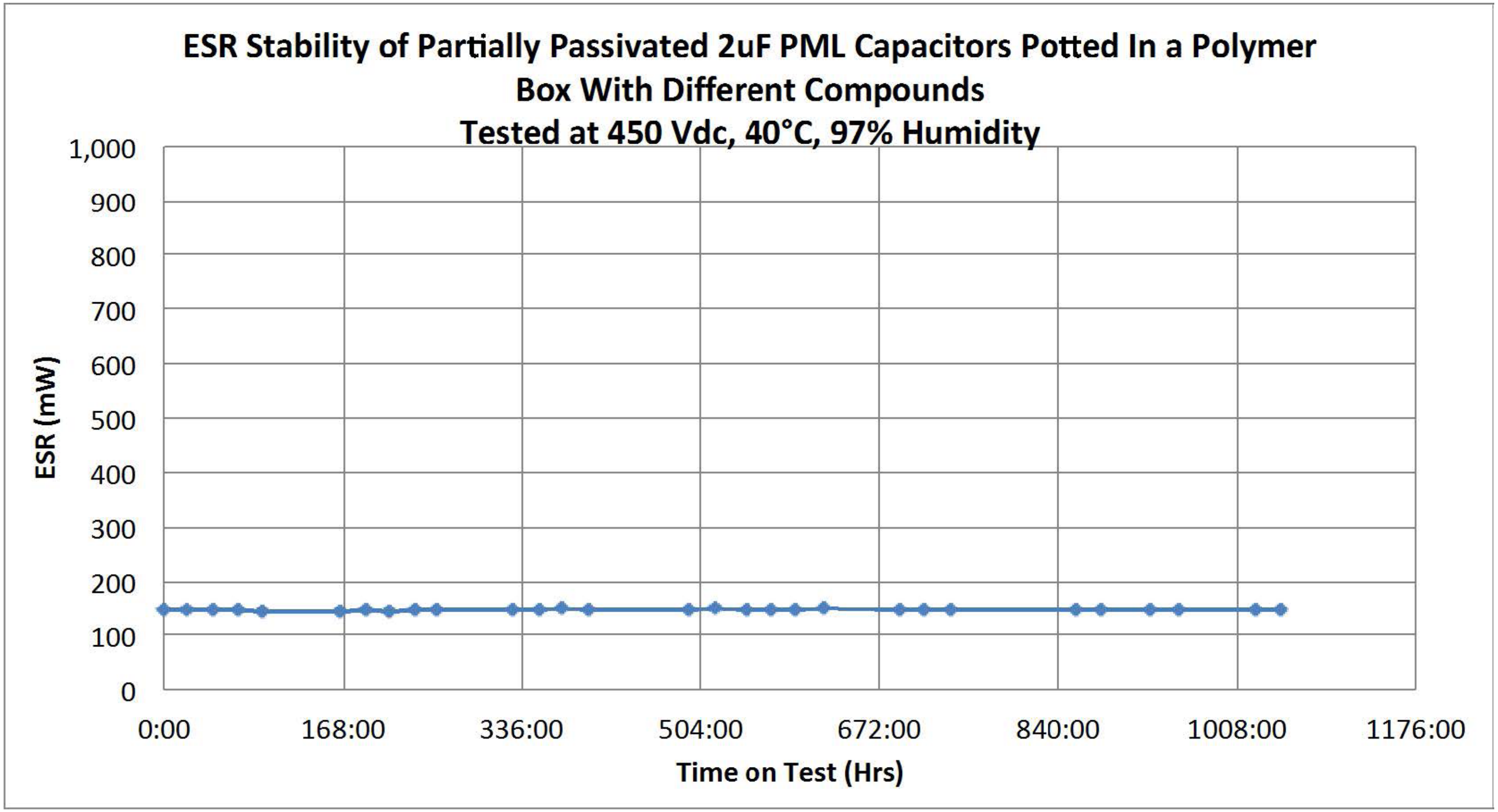
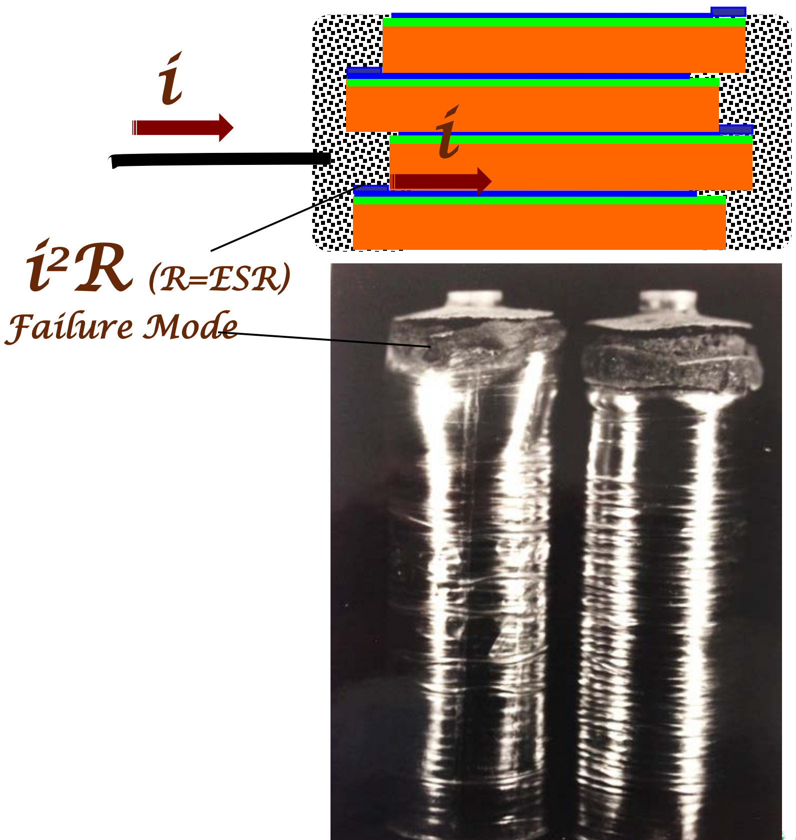
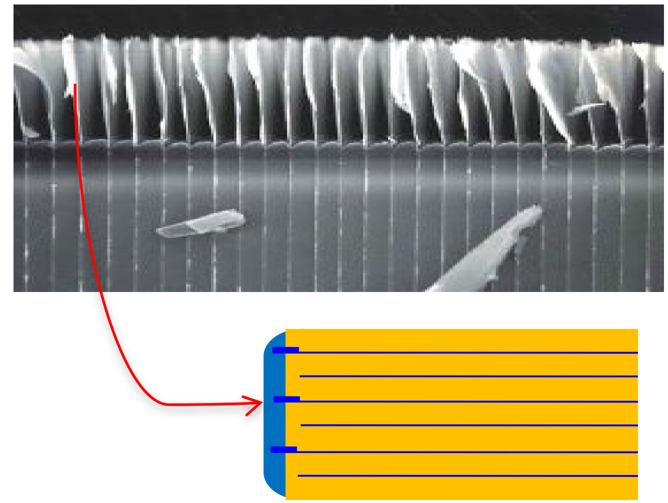
Preliminary Life Test Using a Potting Packaging Process
ESR Stability as Function of Time



Handling of High Ripple Currents and High dV/dt Transients At High Ambient Temperatures, is a Key Requirement For a DC-Link Capacitor

At high ambient temperature >70^{o}C , heat generated from high ripple current in Metallized PP capacitors can lead to loss of contact and higher ESR values, which increases I^2R losses and eventually leads to a catastrophic failure





The PML capacitor dielectric can handle temperatures >250^{o}C

The arc spray makes direct contact with the aluminum electrodes without the presence of polymer that expands and contracts

These factors result in a thermomechanically superior termination that can handle high ripple and dV/dt currents

High Current Termination Combined with a High Temperature Dielectric Lead to Superior Over-Current Performance

Test Capacitors
1000-2000 Layers

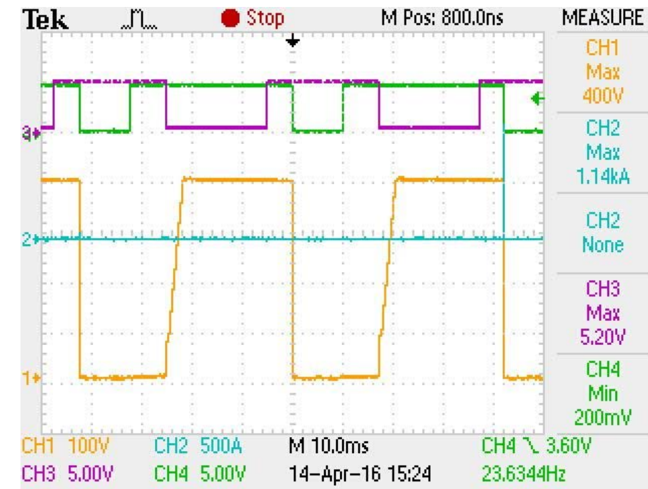
Initial Measurements for Test Capacitor
C_{test} = 2.8uF / 450V
ESR=41mohm

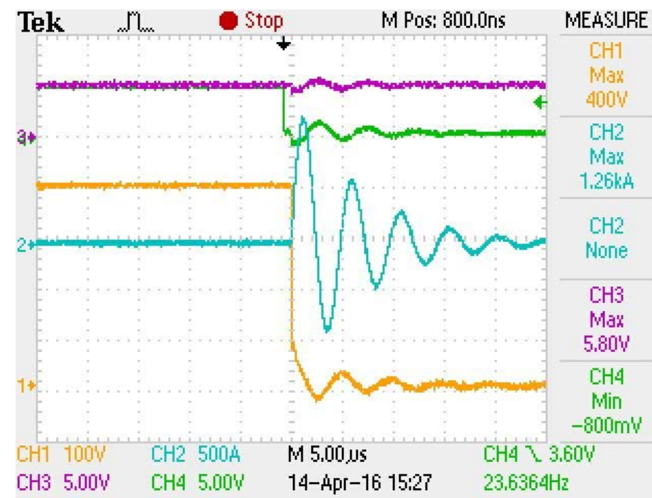
A full size 700uF capacitor will handle 200A rms current
Proportionally, the Test **Capacitor will curry I_{rms}= 0.8A**

After 5000 Pulses at
200V, 600A_{peak}
C_{test}= 2.8uF
ESR = 41mOhm

After 5000 Pulses
300V, 900Apeak
C_{test} =2.8uF
41mOhm

After 5000 Pulses at
400V, 1200A_{peak}
C_{test}=2.8uF
41mOhm
5000 Pulses at
1000X Peak Current
with No Capacitance or ESR Degradation





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Capacitor Specifications and Testing

Delphi has been testing internally series connected sample parts received from Sigma

- Based on the capacitor specifications and life test requirements
- Thermal cycle and thermal storage tests show capacitance and DF within the tolerances of the specification (these are unpackaged parts)
- In near future, packaged parts will be subjected to the bias humidity tests that will indicate ESR change over product life

Thermal Tests and Thermo-Mechanical Modeling

- Thermal imaging was completed for model verification and update on internally connected series capacitors

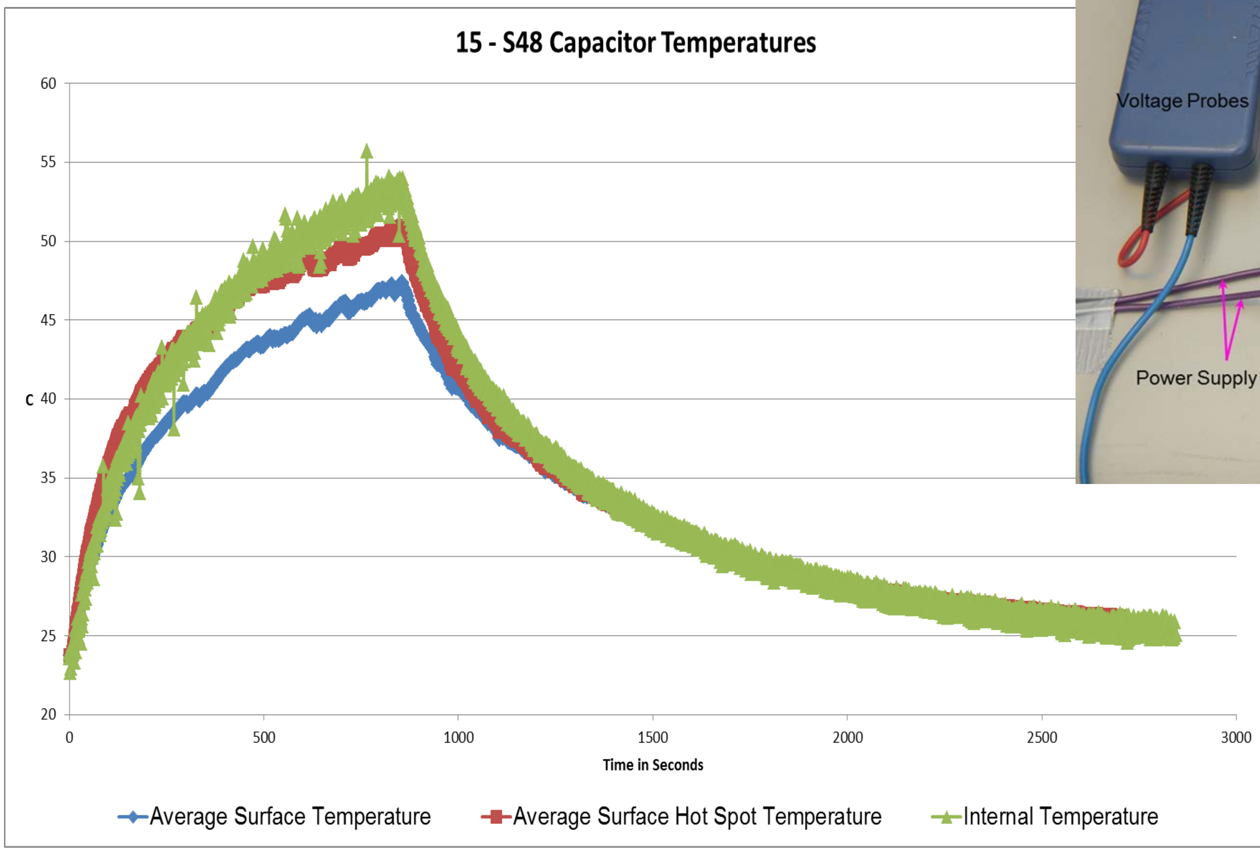
- Testing was completed on un-cooled capacitor stacks comprised of 2, 6, 12, 24 and 48 capacitor strips
  - Capacitor stacks contain an embedded thermistor between the two center capacitor strips of the capacitor stack

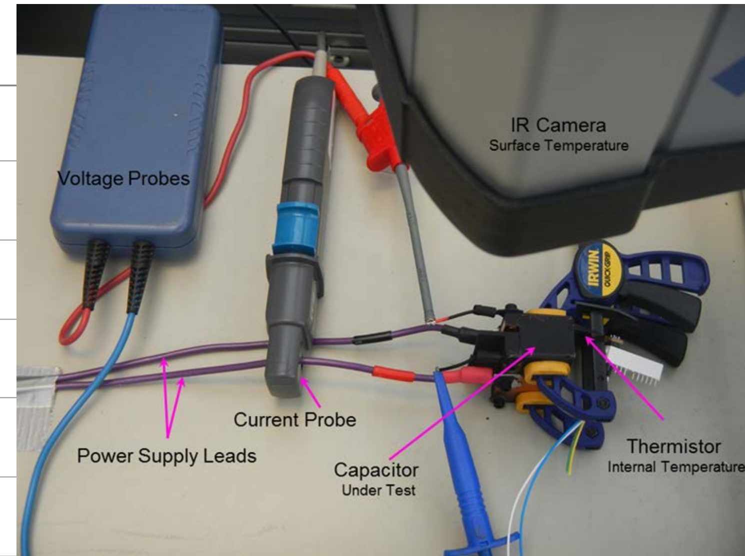
- Surface temperature of the capacitor was measured using an infrared (IR) camera
  - Concurrently temperature at the center of the capacitor stack is measured using the embedded thermistor

- Current used for testing is equivalent to continuous RMS current for the capacitance value under test

- Thermo-mechanical model for internally connected series capacitor is being updated based on test results

Thermal Tests and Thermo-Mechanical Modeling





Response to reviewers comments

Comments from the 2015 Annual Merit Review	Response
This reviewer was concerned that this is a relatively new processing technique for capacitors, and quality control for mass production may require additional research beyond the demonstration scale and low volume production.	High volume production has been demonstrated using production equipment designed and manufactured by Sigma. Lower voltage PML capacitors are produced by the millions and are used in consumer electronic devices
The reviewer believed it would be useful to include more information on what is expected regarding operation life cycle/time of the proposed technology and also some information on the method of determining such information.	Life tests will follow on full size packaged parts
The only item that this reviewer had any concern with was the voltage rating of the part – if 600 Volt would be high enough for potential boosted systems of the future, which will be using 750 to 900 Volt devices and may see a boosted high-voltage bus of 600 to 650 Volt.	Current devices are tested at 720VDC (three internal series). Four internal series will yield 960V and five 1200V.

Collaboration / Coordination with Other Institutions

- Delphi Automotive Systems, LLC
  - U.S.-based Tier 1 supplier to many U.S. and non-U.S. automotive OEMs
  - Delphi has been actively developing inverters and other power electronics products, including battery energy storage systems, for these OEM customers for over 30 years

- Oak Ridge National Laboratory
  - Power Electronics and Electric Machinery Research Center (PEEMRC) is the U.S. Department of Energy's (DOE) premiere broad-based research center for power electronics and electric machinery development
  - The PEEPSRC facilities include state-of-the-art laboratory equipment, and the engineers are versant in a multitude of component and system level modeling programs

Remaining Challenges and Barriers

Can PML capacitors pass the stringent AEC-Q200 Rev D Test Plan?

Preliminary Tests show that

- PML capacitors have low ESR which will minimize I^2R heating
- Current parts perform well under various thermal cycle tests. Performance will improve when parts are packaged
- Parts perform well on DC voltage, dV/dt and current tests
- Preliminary performance on bias/temp/humidity test suggests that packaged passivated PML capacitors will pass this test

At this stage there is not indication that PML capacitors will fail the qualification test plan used to qualify PP capacitors

Future Work

- Rest of FY16
  - Complete packaging design
  - Test packaged Gen2 PML DC-link capacitors according to AEC-Q200 Rev D Test Plan
  - Integrate and test Gen2 PML DC-link capacitors in a Delphi inverter
  - Complete cost analysis and commercialization plan
  - Pursue business plan for transition into production

Summary

Based on capacitor fabrication and testing conducted to date the project is on track to meet and exceed the key target requirements

DC-Link Capacitor Characteristic	DOE Target Requirement	Expected Outcome Based on Test Data
Temperature Range	-40^{o}C to 140^{o}C	-40^{o}C to 140^{o}C
Volume Requirement (liters)	<0.6	<0.3
Direct Cost	<$30	<$20
Failure Mechanism	Safe – Self Healing	Safe – Self Healing
Energy Density	-	3X state of the art metallized PP capacitors
Capacitor Rating	-	400VDC, 600VDC max 700μF, 165A, 295A max

Publications and Presentations

Publications

- None at this time

- A new Patent that includes work funded by the project was recently filed

Presentations

- Sep 2015 – Presented to DOE and Team members
- Feb 2016 – Presented to DOE and Team members