

High Temperature DC-Bus Capacitor Cost Reduction and Performance Improvements

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Sigma Technologies International

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Project ID #: **EDT059**

Overview

High Temperature DC-Bus Capacitors Cost Reduction and Performance Improvements

Timeline

- Start date – October 1, 2013
- End date – April 30, 2016
- Percent complete – 55% as of 3/31/2015

Budget

- Total funding: \$3,510,987
 - DOE share: \$2,288,599
 - Contractor share: \$1,222,338
- Expenditure of DOE funds in
 - FY13: \$129,484
 - FY14: \$1,239,821
 - FY15: \$266,270 (3/31/14)
 - Total: \$1,635,575

Barriers addressed

- A & C (Cost & Weight): Overall size and cost of inverters, as well as thermal management system
- D (Performance and Lifetime): High-temperature operation
 - The performance and lifetime of capacitors available today degrade rapidly with increasing temperature (ripple current capability decreases with temperature increase from 85°C to 105°C)

Partners

- Interactions / collaborations
 - Delphi Automotive Systems
 - Oak Ridge National Laboratory
 - Project lead: Sigma Technologies

Relevance/Objectives

High Temperature DC-Bus Capacitors Cost Reduction and Performance Improvements

- Overall Objectives
 - Reduce the cost, size and weight of the DC-link capacitor by >50%
 - Increase durability in high temperature environments
- Objectives this period
 - Define size and shape of Gen1 capacitor
 - Develop thermal-mechanical and electrical models of the Gen1 capacitor
 - Upgrade pilot line
 - Optimize PML dielectric
- Impact
 - Accelerate the manufacturing capability and mass production adoption of energy-efficient and cost-effective APEEM capacitor technologies into electric drive vehicles, such as electric vehicles (EVs), hybrid electric vehicles (HEVs), and plug-in hybrid electric vehicles (PHEVs)

Project Milestones

High Temperature DC-Bus Capacitors Cost Reduction and Performance Improvements

Month /Year	Milestone or Go /No-Go Decision	Description	Status
Sept 2014	Go/No-Go Decision	Selection of the Gen1 dielectric material with encouraging evaluation of the material's potential to meet or exceed the capacitor targets	Complete
June 2015	Milestone	Completion of the upgrades for the Gen1 prototype capacitor pilot line	On schedule
June 2015	Go/No-Go Decision	Gen1 prototype capacitor testing and evaluation of capacitor performance and the potential of the dielectric material and capacitors to meet or exceed the capacitor targets	On schedule

Approach – Overcome Limitations of Polypropylene (PP) DC-Link Capacitors

High Temperature DC-Bus Capacitors Cost Reduction and Performance Improvements

- Current baseline PP DC-link capacitors are large (~1 liter), heavy (~1 kg), temperature limited (105°C) and costly
 - Metallized PP capacitors must be derated from 85°C to 105°C by at least 30%, which is >50% drop in energy density
 - PP DC-link capacitor supply chain: Today's PP DC-link capacitors utilize extruded and biaxially oriented film produced and metallized by just a handful of film OEMs worldwide, as a result most capacitor OEMs produce similar products and there is limited opportunity for innovation
-
- Sigma has developed a solid state Polymer-Multi-Layer (PML) Having a prismatic shape with
 - low ESL and ESR
 - Operating temperature (T_{op}) range of $-40^{\circ}\text{C} < T_{op} < 140^{\circ}\text{C}$
 - Dielectric constants in the range of $3.0 < k < 6.2$, Dissipation factor $DF < 0.01$
 - Breakdown strength dielectrics
 - Benign failure mode
 - Transformational and potentially disruptive technology: Liquid monomer and Al wire are converted in a single step into Mother Capacitor material

Approach – High Temperature, High energy density Polymer Multi-Layer (PML) DC-Link Capacitors

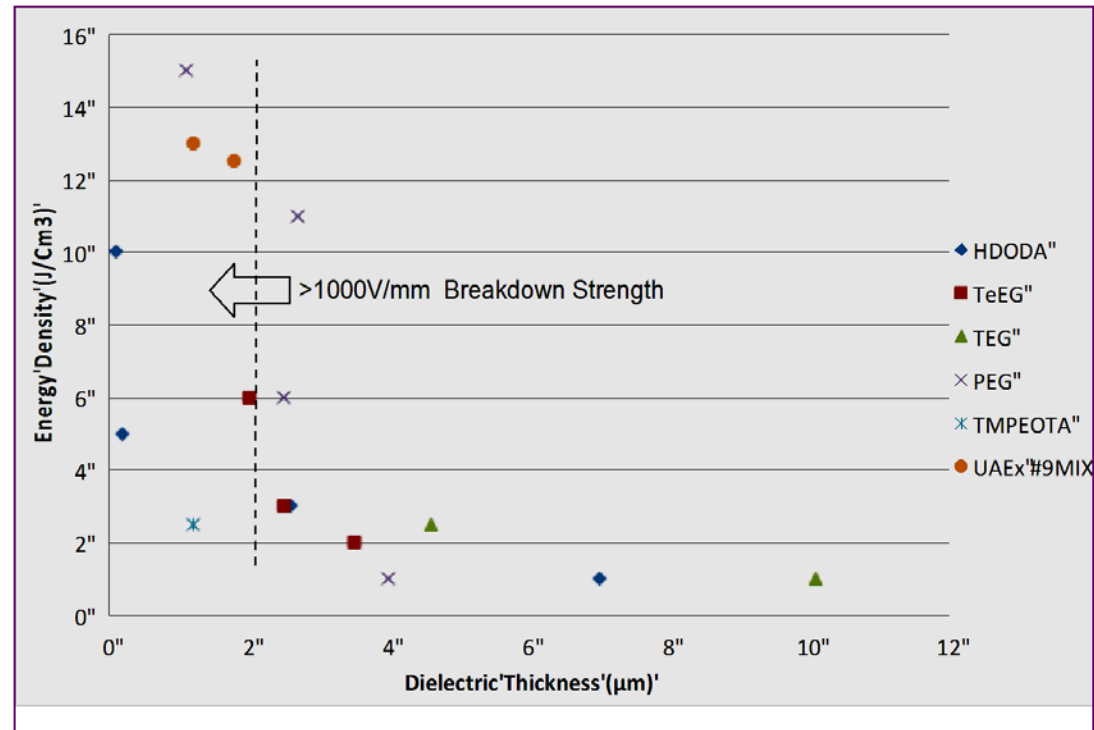
High Temperature DC-Bus Capacitors Cost Reduction and Performance Improvements

Utilize ultrathin dielectrics that have high breakdown strength and produce high energy density capacitors that utilize 2-3 series sections

Develop polymer dielectrics that have a glass transition temperature well above 140°C

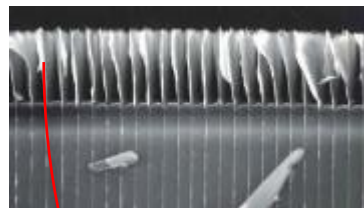
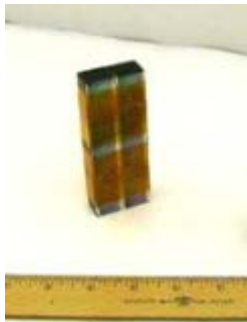
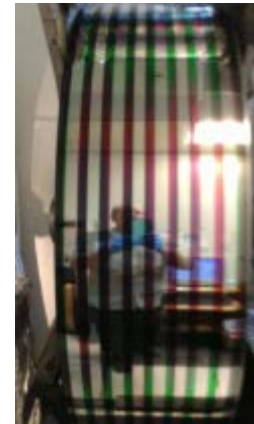
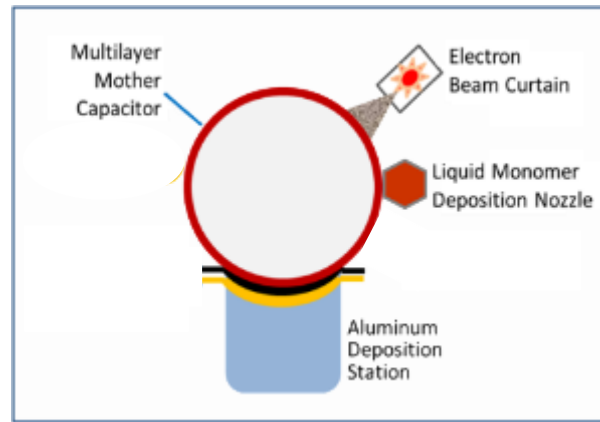
Develop a package that provides adequate protection from moisture, while minimizing capacitor volume and maximizing thermal transfer to the temperature controlled bus bar

Determine thermomechanical material properties of the PML dielectric/electrode composite and develop a predictive thermomechanical model using the projected capacitor geometry, package, electrical contacts and cooling bus bar in the inverter



Approach – High Temperature, High energy density Polymer Multi-Layer (PML) DC-Link Capacitors

High Temperature DC-Bus Capacitors Cost Reduction and Performance Improvements



All aspects of capacitor manufacturing are controlled by the capacitor OEM

Approach – Conformance to Requirements and Reliability

High Temperature DC-Bus Capacitors Cost Reduction and Performance Improvements

Phase I

Sigma addresses conformity to the target Energy Density, DF, ESR and GEN1 product cost by formulating a high temperature dielectric, determining an optimum dielectric thickness, defining electrode resistivity and optimizing various process parameters to assure repeatability in producing capacitor samples

Delphi tests parts to verify their conformance to basic requirements extracted from test methodology that is place for DC-Link capacitors used in inverters

Delphi measures material properties of the PML capacitors including: CTE, Tg, Heat Capacity, Thermal Diffusivity, Thermal Conductivity, Density, Glass Transition Temperature Storage Modulus and Tan δ

Oak Ridge National Labs (ORNL), utilizes material properties and to construct a generic thermo-mechanical model of the capacitor to predict thermal performance over various drive cycles as well as evaluating different packaging options to maximize thermo-mechanical reliability of the PML DC-link capacitor.

Approach – Conformance to Requirements and Reliability (cont'd)

High Temperature DC-Bus Capacitors Cost Reduction and Performance Improvements

Phase II

Sigma optimizes manufacturing processes to address thermo-mechanical reliability issues resulting from process the include the arc sprayed termination and high temperature heat setting of the capacitor stack

Sigma revisits conformity to energy density and product cost by making potential improvements to the capacitor dielectric

Delphi tests capacitors in accordance with a subset of the automotive Passive Component Qualification Test Plan to assure conformance to requirements and reliability

A capacitor will be installed into an existing inverter or power stage for system testing using an inductive load and a motor load on a dyne and the DC-link capacitor performance will be measured, characterized and documented.

ORNL will update the thermo-mechanical model using the GEN2 capacitor geometry, package and electrical contacts

Approach - Technology To Market Plan: PML Capacitor Commercialization

High Temperature DC-Bus Capacitors Cost Reduction and Performance Improvements

- Working on funding a Sigma PML capacitor spinoff operation
 - Have supplied PML capacitors for evaluation to a potential strategic partner
- Considering licensing one or more major capacitor OEMs to create at one additional product source
 - Have supplied PML parts to interested parties for preliminary evaluation of the basic capacitor properties as they relate to inverter applications
- Exploring other capacitor applications that have lesser qualification requirements

Technical Accomplishments

Requirements and Process Tradeoffs

High Temperature DC-Bus Capacitors Cost Reduction and Performance Improvements

- Automotive requirements vary for different EDV applications which typically change the requirements for the DC-link capacitor
- Delphi has seen EDV inverter requirements that require DC-link capacitance anywhere between 300 μF to 1200 μF for a given application
 - Delphi has supplied Sigma with requirements for a family of DC-link capacitors
- Delphi has been working with Sigma to define an optimal shape for producing DC-link capacitors using their PML process
 - Number of layers (capacitors in parallel) is equivalent to the number of times the PML process drum goes around and around
 - By fixing the area the tooling for these various capacitor values becomes common
 - By fixing the capacitor area, the capacitor height can be increased or decreased for different values of capacitance
 - Fixing the area and varying the number of layers (volume) helps to lower the cost of the DC-link capacitor

Technical Accomplishments – Pilot Line Upgrades

High Temperature DC-Bus Capacitors Cost Reduction and Performance Improvements

Capacitor Machine



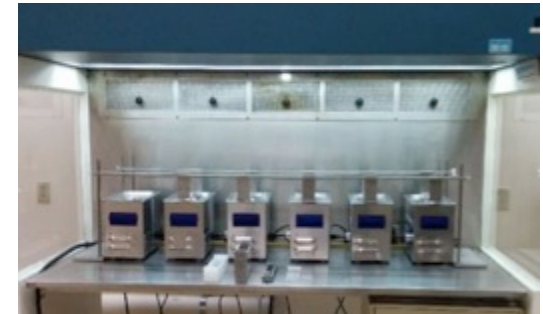
Heat Setting



Dicing



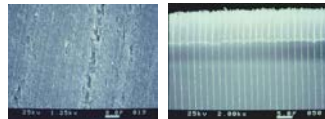
Etching



Inline Passivation



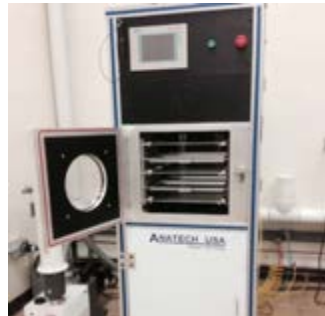
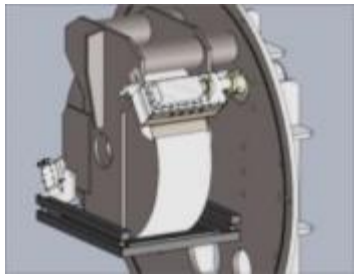
Plasma Ashing



Termination Arc Spray



Life Test Equipment



Technical Accomplishments – Inline Passivation Of Capacitor Electrodes

High Temperature DC-Bus Capacitors Cost Reduction and Performance Improvements

A plasma reactor was built to passivate the aluminum electrodes in-line with the deposition process

400KHz and 13.5MHz plasma power was used along with a variety of plasma gases to produce different passivation conditions

An accelerated corrosion test
Involving high pressure steam was
used to determine the best
passivation process



Poor Passivation



Good Passivation

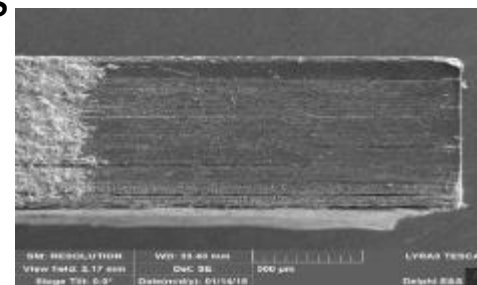
A set of conditions was developed that provides adequate passivation for the GEN1 PML capacitors

Technical Accomplishments – Plasma Ashing to Reveal the Aluminum Electrodes

High Temperature DC-Bus Capacitors Cost Reduction and Performance Improvements

A series of experiments were conducted to develop an optimal set of plasma ashing conditions. Experiments included:

- ❖ Ashing rate as a function of plasma gas – An Argon oxygen mixture was selected as the most effective
- ❖ Plasma Power – Various power levels were tested to minimize ashing time while preventing arcing
- ❖ Pressure during the ashing process – Pressure affects ashing rate, ashing uniformity and temperature of parts during the ashing process
- ❖ Thermocouples were placed on the parts and the temperature during ashing was as high as 260°C. Layer separation was observed

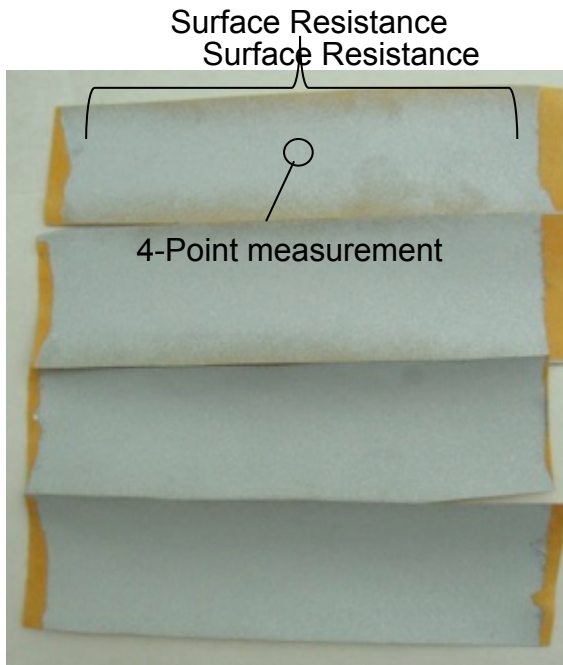


**Plasma power and pressure were adjusted to keep temperature <240°C
a heat setting process is put into place to prebake the parts at 240°C**

Technical Accomplishments – Arc Spraying to Terminate the Plasma Ashed Electrodes

High Temperature DC-Bus Capacitors Cost Reduction and Performance Improvements

A series of experiments were conducted to determine an optimum set of conditions for the capacitor termination process. Experiments included different metal sprays, arc current, spray distance and gas flow.



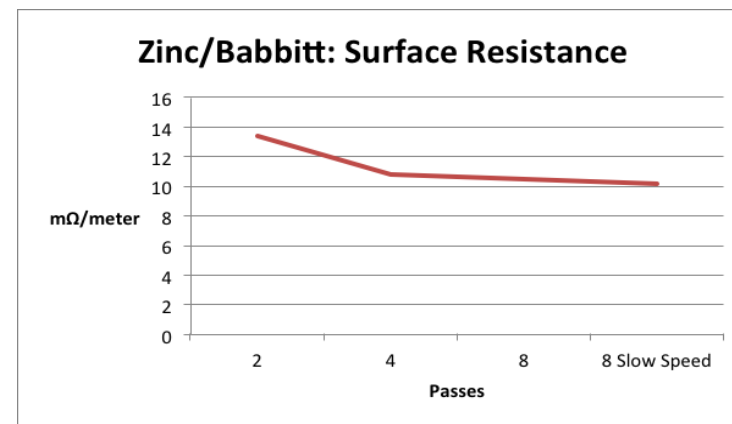
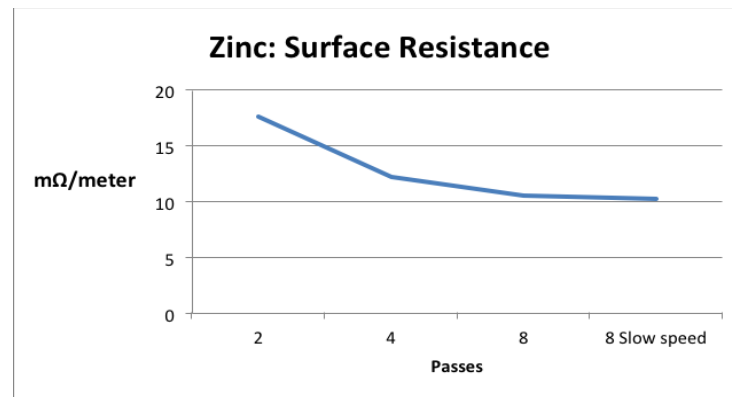
Zinc Metal Spray

Spray Gun Height	Passes	Surface Resistance miliOhm/cm
17.0	2	>10
17.0	4	1.97
17.0	8	0.29
10.0	2	4.75
10.0	4	0.87
10.0	8	0.50
5.0	2	3.50
5.0	4	1.25
5.0	8	0.62

Technical Accomplishments – Arc Spraying to Terminate the Plasma Ashed Electrodes – Cont.

High Temperature DC-Bus Capacitors Cost Reduction and Performance Improvements

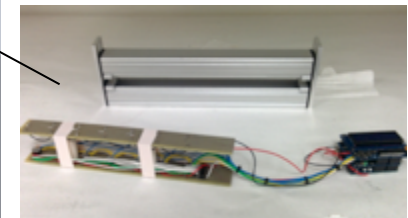
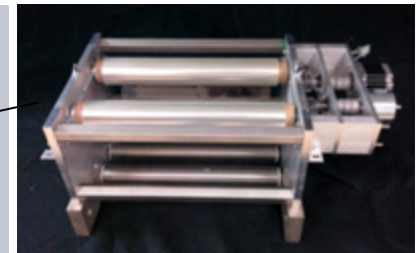
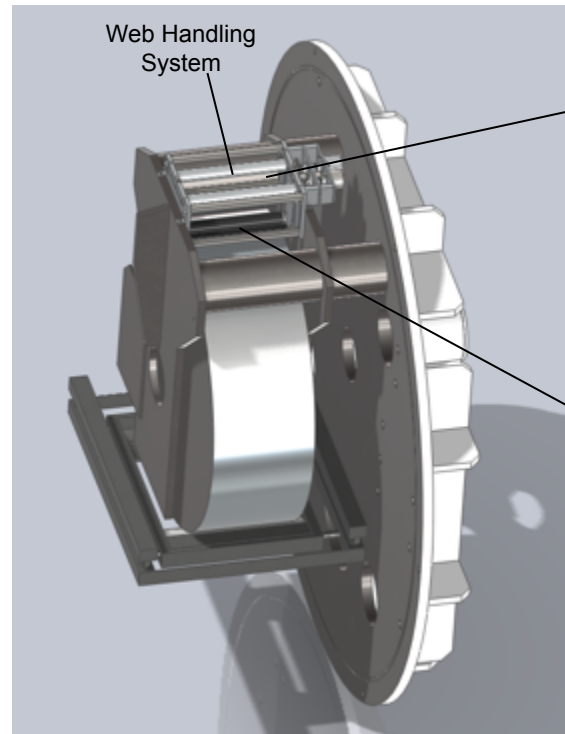
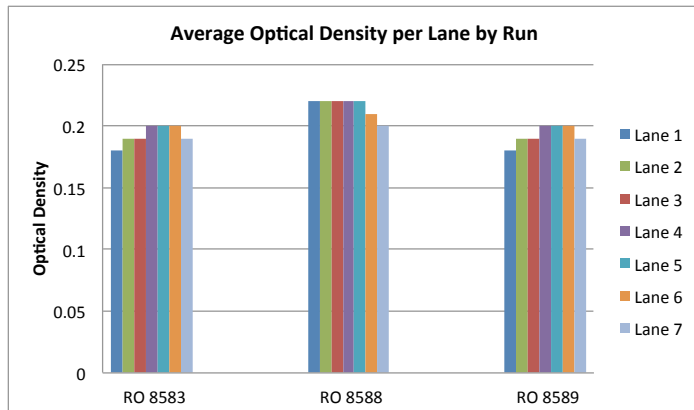
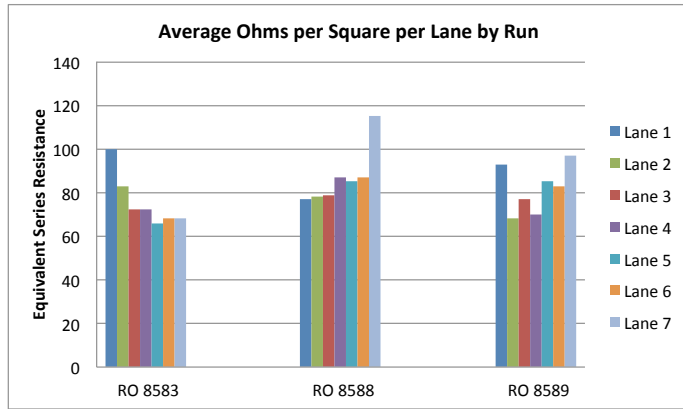
Zinc Spray Gun Height (cm)	Passes	Resistivity (4 point) miliOhm/Sq	Surface Resistance miliOhm/cm
17	2	17.7	>10
17	4	17.6	1.97
17	8	17.7	0.29
Zinc/Babbitt Spray Gun Height (cm)			
17	2	17.6	3.14
17	4	17.2	0.59
17	8	17.0	0.29
Aluminum Spray Gun Height			
17	2	N/A	N/A
17	4	19	354
17	8	18.9	4.3



Zinc and / or Babbitt are chosen for the Capacitor Termination Process

Technical Accomplishments – Inline Control of Electrode Resistivity

High Temperature DC-Bus Capacitors Cost Reduction and Performance Improvements



The electrode resistivity which impacts capacitor self healing process, will be controlled using an inline optical densitometer

Technical Accomplishments – Optimization of PML Dielectric for Gen1 Capacitor

High Temperature DC-Bus Capacitors Cost Reduction and Performance Improvements

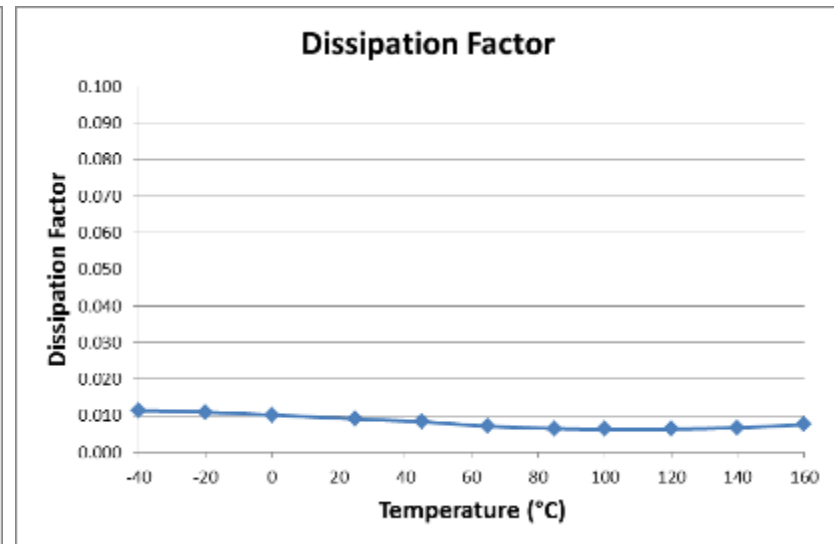
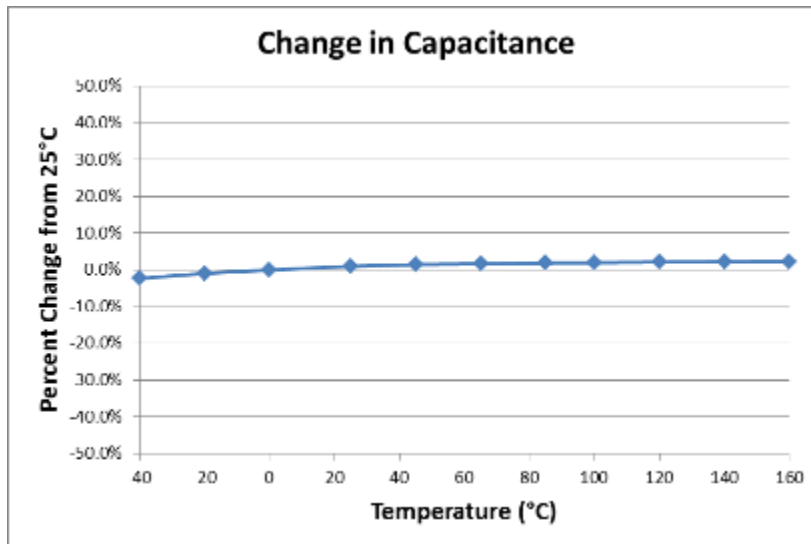
Key variables taken into consideration when optimizing the polymer dielectric and capacitor electrodes include:

- Breakdown strength
- Self healing properties
- Energy density
- Mechanical properties as they impact capacitor processing and self-healing
- Ease of flash evaporation
- Capacitance stability with temperature up to 140°C
- Dissipation Factor stability up to 140°C with an upper limit <0.01

Technical Accomplishments – Optimization of PML Dielectric for Gen1 Capacitor (cont'd)

High Temperature DC-Bus Capacitors Cost Reduction and Performance Improvements

Capacitance and Dissipation Factor Stability of GEN1 Dielectric
2000 layers 0.65 μm Thick Layers, Cap=32 μF , Dielectric Constant 3.2

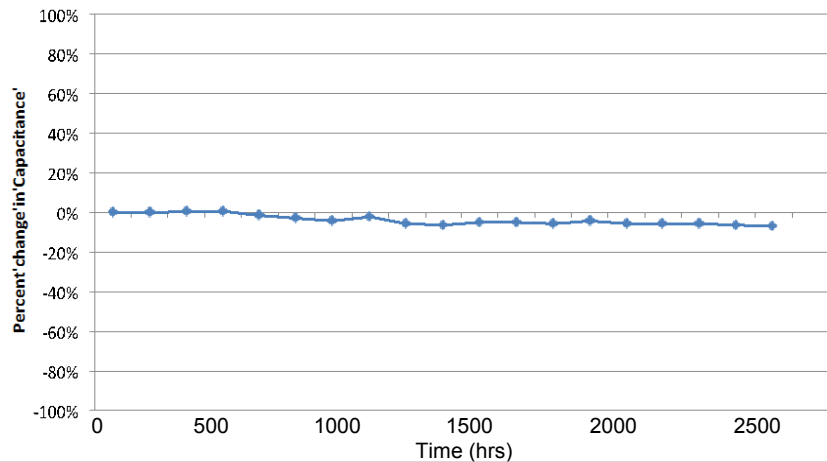


**A self healing thermally stable polymer dielectric was developed
with a glass transition temperature $T_g > 180^\circ\text{C}$**

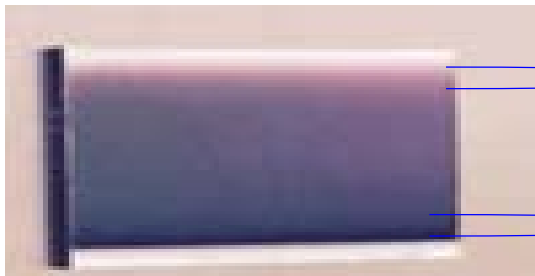
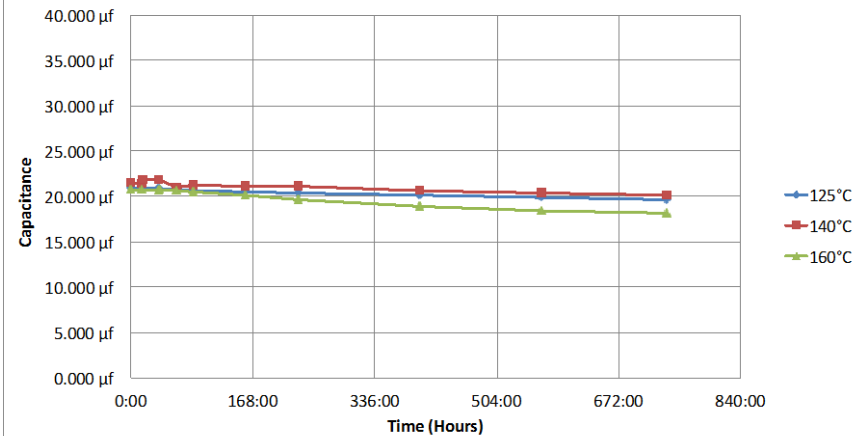
Technical Accomplishments – Life test of PML Capacitors

High Temperature DC-Bus Capacitors Cost Reduction and Performance Improvements

Life Test Condition 150V (3X=450V) and 125°C



Average Change of Capacitance as a Function of Time (8 parts per condition)
Parts Tested at 150VDC and Different Ambient Temperatures



Graded electrode edge due to the shadow mask is effectively 15% to 20% of the total electrode area and contributes to capacitance loss. Steps are taken to reduce the graded electrode to 1-2% of the capacitor area

Technical Accomplishments – Demonstration of Breakdown Strength of the Thin Polymer Dielectrics used in GEN1 PML Capacitors

High Temperature DC-Bus Capacitors Cost Reduction and Performance Improvements

RECORD ENERGY DENSITY FOR A POLYMER DIELECTRIC CAPACITOR **770V/ μm on 13 μF Capacitor**

Dielectric Thickness 0.65 μm

Dielectric constant 3.2

1000 layers

Applied Voltage with no degradation 500V

Energy Density of active capacitor 8J/cc

Energy Density of actual capacitor 4.5J/cc (this can be significantly improved)

Capacitors lost 5% capacitance at 600VDC (**924V/ μm 11.5 J/cc active 6.5 J/cc capacitor**)

These results demonstrate the >1000V/ μm intrinsic breakdown strength of the PML capacitor dielectrics

Technical Accomplishments – Energy Density of GEN1 Capacitors

High Temperature DC-Bus Capacitors Cost Reduction and Performance Improvements

ENERGY DENSITY OF GEN1 PML CAPACITORS TARGET: 3X ENERGY DENSITY OF MPP CAPACITORS Dielectric Thickness 0.65 μ m

	GEN1 Rating $V_{\text{rated}} = 150\text{V}$ 3X=450V	Potential GEN2 $V_{\text{rated}} = 175\text{V}$ 3X=525V
Hipot Voltage 240V (3X=720V)		
Energy Density of Individual Capacitors (J/cc)*	0.59	0.80
Energy Density of Three Capacitors in Series (J/cc)**	0.49	0.65

* Capacitors as currently produced

** Energy density of packaged DC-Link Capacitor

**Energy density of current metallized PP capacitors used by Delphi is about 0.1 J/cc
PML capacitor will achieve the target 3X reduction in capacitor volume**

Technical Accomplishments – Material Properties

High Temperature DC-Bus Capacitors Cost Reduction and Performance Improvements

Sigma has provided three sets of PML capacitor samples to Delphi for testing at different stages of the development

First two sets have:

- Active Width x Active Length = 16.5 mm x 25.4 mm
- 1000 active layers, active area thickness 1 mm
- With 200 top and 200 bottom passive layers of 0.65 μm /layer dielectric, dielectric constant 3.2
- Not passivated (some were partially passivated, baked), un-packaged

Third set, recently provided, is fully passivated with 1500 active layers, and 30 passive layers top and 30 layers bottom

- Currently under test

In general, these capacitance/volume results are very good compared to PP
Partially passivated parts perform better than un-passivated parts
Fully passivated should perform better than partially passivated

Technical Accomplishments – Thermo-mechanical Model

High Temperature DC-Bus Capacitors Cost Reduction and Performance Improvements

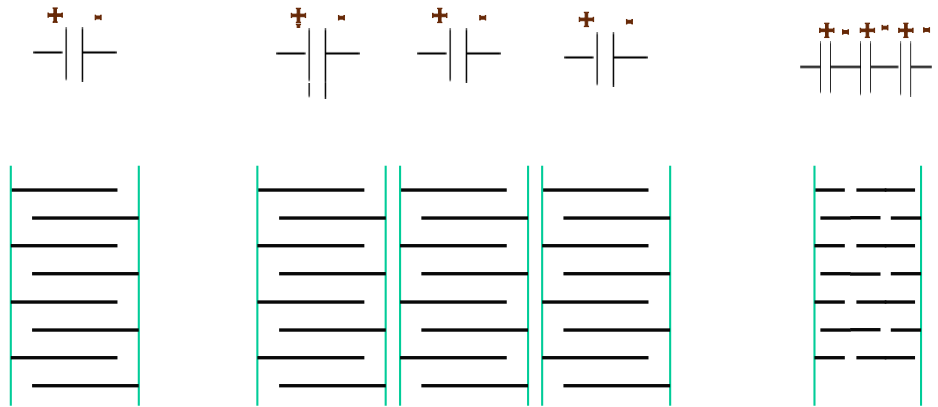
- **Delphi working with Sigma and ORNL is investigating three possible configurations for a DC-link capacitor**
 - Based on processing steps, potential yields, electrical, thermal and mechanical performance
- **Thermal limitations will define the maximum ESR for the capacitor**
 - The Sigma dielectric material has a $T_g > 180^\circ\text{C}$
 - Delphi will work with Sigma to determine the maximum continuous thermal rating of the capacitor, based on the maximum continuous rated ripple current
 - Allowable Δt is somewhere between 90°C and 110°C (180°C continuous rating – 70°C heat rail)
 - Compares with a Δt of $\sim 30^\circ\text{C}$ for PP (100°C continuous rating – 70°C heat rail)
 - » 85°C rating for PP with a 15°C internal temp rise gives the 100°C continuous rating
- **Using models developed by ORNL, Delphi will investigate the maximum heat flux the DC-link capacitor can withstand**
 - Delphi heat rail, gap pad, ... applied to ORNL model
 - Configuration 1 - Externally connected DC-link capacitor
 - Configuration 2 - Internally connected DC-link capacitor (shadow mask)
 - Configuration 3 - Internally connected DC-link capacitor (using new mask that reduces graded edge)
 - Potentially best thermal and energy density

Technical Accomplishments – Capacitor Design to Maximize Volumetric Efficiency and Minimize ESR

High Temperature DC-Bus Capacitors Cost Reduction and Performance Improvements



Current parts 20mm x 25mm
1000-2000 layers with various ESR values
Maximum applied 240V (3x= 720V)



Final part design 20mm x 125mm
2000 – 3000+ layers

A new mask will be used to eliminate the graded electrode edge resulting from the shadow mask

Three capacitors connected internally in series

These parts will have 1/3 of the ESR of current parts for the same ohm/sq electrodes

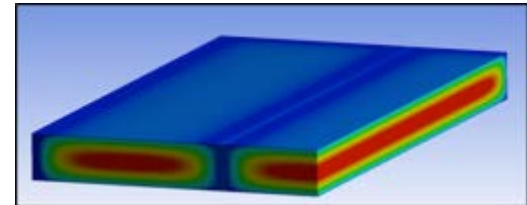
Technical Accomplishments – Thermo-mechanical Model

High Temperature DC-Bus Capacitors Cost Reduction and Performance Improvements

Modeling - ORNL

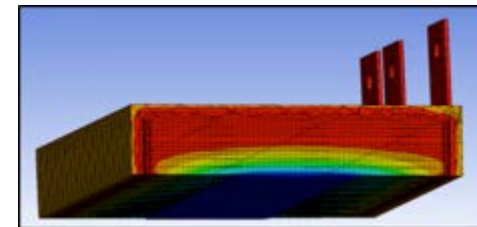
- **Thermal and thermo-mechanical modeling (ANSYS)**
 - Iteratively provide results to Delphi/Sigma to contribute to their DC-link capacitor design refinements
 - Estimate maximum temperatures and temperature gradients produced from ESR losses
 - Estimate maximum stresses and their locations within the DC-link capacitor designs and interpret their potential to compromise mechanical reliability
- **Assistance with property measurements**
 - Flash diffusivity to determine anisotropic thermal response of multi-laminate capacitor structure
 - Property measurements fed back into above modeling

CONCEPT 1 EXAMPLE



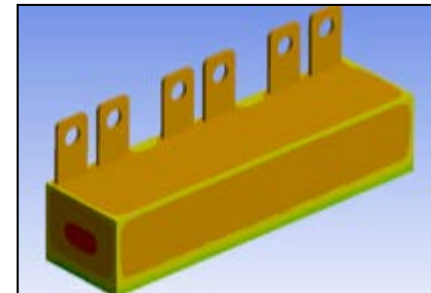
Arbitrary Temperature Profile (one-quarter model)

CONCEPT 2 EXAMPLE



Arbitrary Temperature Profile (one-half model)

CONCEPT 3 EXAMPLE



Arbitrary Temperature Profile (whole model)

Response to reviewers comments

High Temperature DC-Bus Capacitors Cost Reduction and Performance Improvements

Comments from the 2014 Annual Merit Review	Response
<i>The reviewer also mentioned that the project proposed to use plasma etching to assist in the end connections, so it will be very interesting to this reviewer to see the test results as plasma may remove both the polymer and the thin metallization.</i>	This process is best described as “plasma ashing” which works by using an oxygen plasma to “ash” or “burn” the polymer by converting it to CO, CO ₂ , ethane, methane, and other gases. The aluminum electrodes are protected by the formation of a thin Al ₂ O ₃ passivating layer that is only 10-15A thick.
<i>The reviewer offered that it seemed like it would be helpful to have a capacitor manufacturer involved.</i>	At this stage of the development Sigma has all the process and equipment technology knowhow to execute the project. At least one multinational capacitor OEM will be involved at a later stage
<i>The reviewer also stated that high-voltage performance may also be a challenge, as the other two ends would be cut with a diamond saw and there may be a corona around the edges without un-metallized margins.</i>	Corona is not present in DC-Link capacitors, unless the ripple current voltage exceeds 200VAC

Collaboration / Coordination with Other Institutions

High Temperature DC-Bus Capacitors Cost Reduction and Performance Improvements

- Delphi Automotive Systems, LLC
 - U.S.-based Tier 1 supplier to many U.S. and non-U.S. automotive OEMs
 - Delphi has been actively developing inverters and other power electronics products, including battery energy storage systems, for these OEM customers for over 30 years
- Oak Ridge National Laboratory
 - Power Electronics and Electric Machinery Research Center (PEEMRC) is the U.S. Department of Energy's (DOE) premiere broad-based research center for power electronics and electric machinery development
 - The PEEPSRC facilities include state-of-the-art laboratory equipment, and the engineers are versant in a multitude of component and system level modeling programs

Remaining Challenges and Barriers

High Temperature DC-Bus Capacitors Cost Reduction and Performance Improvements

Phase I

- Will the pilot line upgrade be completed on time to produce and evaluate the performance of 800 μF / 400V / 600V_{transient} DC-link capacitors
 - All the originally proposed pilot line improvements have already been completed. Sigma is working on some additional improvements that were identified during the Phase I project.
- Can PML Gen1 capacitors meet the projected improvements in thermomechanical performance and energy density?
 - Data suggests that PML capacitors will achieve and probably exceed the proposed performance targets

Phase II

- Can PML Gen2 capacitors pass the stringent AEC-Q200 Rev D Test Plan?
 - Like all metallized capacitors an effective package will be required to protect the aluminum electrodes from exposure to humidity at high temperatures

Future Work

High Temperature DC-Bus Capacitors Cost Reduction and Performance Improvements

- Rest of FY15
 - Complete additional pilot line improvements
 - Complete package design and evaluate packaged Gen1 capacitors
 - Preliminary cost analysis and commercialization plan
 - Develop Gen2 capacitors
 - Package and evaluate Gen2 capacitors
 - Develop business plan
- FY16
 - Test packaged Gen2 PML DC-link capacitors according to AEC-Q200 Rev D Test Plan
 - Integrate and test Gen2 PML DC-link capacitors in a Delphi inverter
 - Complete cost analysis and commercialization plan
 - Pursue business plan for transition into production

Summary

High Temperature DC-Bus Capacitors Cost Reduction and Performance Improvements

Based on capacitor fabrication and testing conducted to date the project is on track to meet and exceed the key target requirements

DC-Link Capacitor Characteristic	DOE Target Requirement	Expected Outcome Based on Test Data
Temperature Range	-40°C to 140°C	-40°C to 140°C
Volume Requirement (liters)	<0.6	<0.3
Direct Cost	<\$30	<\$20
Energy Density	-	>2X state of the art metallized PP capacitors
Capacitor Rating	-	430VDC, 600VDC max 700μF, 165A, 295A max

Project is on track to transition into the Phase II