

High Temperature DC-Bus Capacitor Cost Reduction and Performance Improvements

Angelo Yializis

Sigma Technologies International

6/17/2014

Project ID #: **APE059**

Overview

High Temperature DC-Bus Capacitors Cost Reduction and Performance Improvements

Timeline

- Start date – October 1, 2013
- End date – January 31, 2016
- Percent complete – 10% as of 3/31/2014

Budget

- Total funding: \$3,510,987
 - DOE share: \$2,288,599
 - Contractor share: \$1,222,338
- Expenditure of DOE funds in
 - FY13: \$0
 - FY14: \$251,650 (10/13-3/31/14)
 - Total

Barriers addressed

- A & C (Cost & Weight): Overall size and cost of inverters, as well as thermal management system
- D (Performance and Lifetime): High-temperature operation
 - The performance and lifetime of capacitors available today degrade rapidly with increasing temperature (ripple current capability decreases with temperature increase from 85°C to 105°C)

Partners

- Interactions / collaborations
 - Delphi Automotive Systems
 - Oak Ridge National Laboratory
 - Project lead: Sigma Technologies

Relevance/Objectives

High Temperature DC-Bus Capacitors Cost Reduction and Performance Improvements

- Overall Objectives
 - Reduce the cost, size and weight of the DC-link capacitor by >50%
 - Increase durability in high temperature environments
- Objectives this period
 - Define size and shape of Gen1 capacitor
 - Develop thermal-mechanical and electrical models of the Gen1 capacitor
 - Upgrade pilot line
 - Optimize PML dielectric
- Impact
 - Accelerate the manufacturing capability and mass production adoption of energy-efficient and cost-effective APEEM capacitor technologies into electric drive vehicles, such as electric vehicles (EVs), hybrid electric vehicles (HEVs), and plug-in hybrid electric vehicles (PHEVs)

Project Milestones

High Temperature DC-Bus Capacitors Cost Reduction and Performance Improvements

Month /Year	Milestone or Go /No-Go Decision	Description	Status
June 2014	Go/No-Go Decision	Selection of the Gen1 dielectric material with encouraging evaluation of the material's potential to meet or exceed the capacitor targets	On schedule
Oct 2014	Milestone	Completion of the upgrades for the Gen1 prototype capacitor pilot line	On schedule
March 2015	Go/No-Go Decision	Gen1 prototype capacitor testing and evaluation of capacitor performance and the potential of the dielectric material and capacitors to meet or exceed the capacitor targets	On schedule

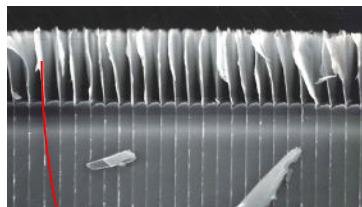
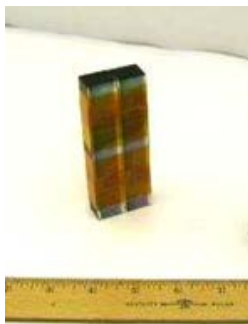
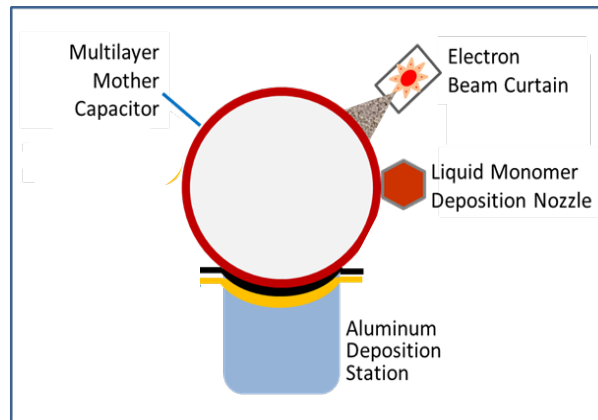
Approach – Overcome Limitations of Polypropylene (PP) DC-Link Capacitors

High Temperature DC-Bus Capacitors Cost Reduction and Performance Improvements

- Current baseline PP DC-link capacitors are large (~1 liter), heavy (~1 kg), temperature limited (105°C) and costly
 - Metallized PP capacitors must be derated from 85°C to 105°C by at least 30%, which is >50% drop in energy density
- PP DC-link capacitor supply chain
 - Today's PP DC-link capacitors utilize extruded and biaxially oriented film produced and metallized by just a handful of film OEMs worldwide
 - The metallized PP film is then distributed to 100s of capacitor OEMs who wind, test, and package DC-link capacitors, that are supplied to the inverter OEMs
 - Capacitor OEMs have no control of the PP dielectric; instead they can specify and control:
 - Width and length of the capacitor
 - Wound round vs. wound flat and stacked parts
 - Metallized electrode thickness and design
 - Capacitor package
 - As a result most capacitor OEMs produce similar products and there is limited opportunity for innovation

Approach – Proposed Polymer Multi-Layer (PML) DC-Link Capacitors

High Temperature DC-Bus Capacitors Cost Reduction and Performance Improvements



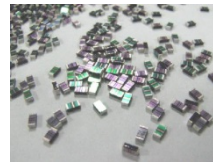
All aspects of capacitor manufacturing are controlled by the capacitor OEM

Approach – Produce Higher Voltage PML Capacitors

High Temperature DC-Bus Capacitors Cost Reduction and Performance Improvements

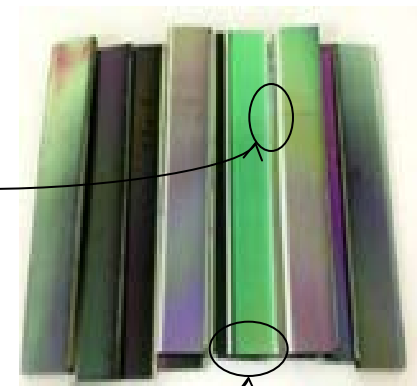
- PML capacitors are commercially available for low-voltage, surface-mount consumer electronic applications

(produced by Sigma licensees)



PML Chip compared to MKT type film capacitor (35v 10 μ F)

- Sigma has developed a new generation, higher voltage PML capacitors by:
 - Integrating a heavy edge in the multilayer stack, which allows much higher ohm/sq in the active area
 - Eliminating the electrode at the cut edge, thus eliminating surface flash-over



Approach – Conformance to Requirements and Reliability

High Temperature DC-Bus Capacitors Cost Reduction and Performance Improvements

Phase I

- Delphi will work with Sigma on capacitor requirements (electrical, mechanical and test), packaging options and process capabilities
- Sigma will provide sample functional capacitors for Delphi for testing to verify their conformance to requirements
- Delphi will also measure the material properties of the individual materials that make up the capacitor
 - For example: CTE, T_g, Heat Capacity, Thermal Diffusivity, Thermal Conductivity, Density, Storage Modulus, Tan δ , among others
- Delphi will provide these material properties to Oak Ridge National Labs (ORNL), where these properties will be used to construct a generic thermo-mechanical model of the capacitor
 - The model will be used to predict the performance of the capacitor over various drive cycles and environmental conditions for the life of the capacitor as well as evaluating different packaging options to make a thermally and mechanically reliable DC-link capacitor. This model will be verified and updated over time.

Approach – Conformance to Requirements and Reliability (cont'd)

High Temperature DC-Bus Capacitors Cost Reduction and Performance Improvements

Phase II

- Sigma will provide Delphi form, fit and functional capacitors for testing.
- Delphi will test the capacitors to verify conformance to requirements
 - Delphi will also test some of the capacitors in accordance with a subset of the automotive Passive Component Qualification Test Plan
 - Delphi will also install a capacitor into an existing inverter or power stage for system testing using an inductive load and a motor load on a dyne and the DC-link capacitor performance will be measured, characterized and documented.
- Delphi will continue to work with ORNL to update the thermo-mechanical model as needed

Technical Accomplishments – Requirements and Process Tradeoffs

High Temperature DC-Bus Capacitors Cost Reduction and Performance Improvements

- Automotive requirements vary for different EDV applications which typically change the requirements for the DC-link capacitor
- Delphi has seen EDV inverter requirements that require DC-link capacitance anywhere between 300 μF to 1200 μF for a given application
 - Delphi has supplied Sigma with requirements for a family of DC-link capacitors
- Delphi has been working with Sigma to define an optimal area for producing DC-link capacitors using their PML process
- By fixing the capacitor area, the capacitor height can be increased or decreased for different values of capacitance
 - Number of layers (capacitors in parallel) is equivalent to the number of times the PML process drum goes around and around
 - By fixing the area the tooling for these various capacitor values becomes common
- Fixing the area and varying the number of layers (volume) helps to lower the cost of the DC-link capacitor

Technical Accomplishments – Material Properties

High Temperature DC-Bus Capacitors Cost Reduction and Performance Improvements

- Delphi, using dielectric materials supplied by Sigma, is measuring their material properties
- These measurements, along with others, have been supplied to ORNL for inclusion into their model
- Heat capacity was determined by running modulated digital scanning calorimeter (DSC) experiment on a sample of the resin
 - From this, C_p is determined and multiplied by a calibration correction factor at selected temps
 - The calibration factor, $K C_p$ is determined by running the same experiment on sapphire, with a known C_p over a large temperature range
- Delphi has also measured the thermal diffusivity of a metallized and non-metallized dielectric samples
 - Using the measured density of the material and the C_p , the thermal conductivity was calculated

Sigma Acrylate-based Material

Temp (°C)	C_p uncorrected J/g°C	K C_p Correction factor	C_p Corrected J/g°C
26.8	.93	.89	.83
46.8	.98	.92	.90
66.8	1.03	.94	.97
86.8	1.07	0.97	1.04
106.8	1.11	1.00	1.11
126.8	1.14	1.03	1.17
146.8	1.17	1.06	1.24

Temperature (°C)	Thermal Conductivity (W/mK)	Thermal Resistance (cm ² , °C/W)	Thermal Diffusivity (cm ² /s)
20	0.14	41	0.0012
100	0.17	34	0.0011

Sigma Composite #8379

Temperature (°C)	Thermal Conductivity (W/mK)	Thermal Resistance (cm ² , °C/W)	Thermal Diffusivity (cm ² /s)
20	0.27	3.3	0.0011
100	1.27	0.7	0.0015

Technical Accomplishments – Thermo-mechanical Model

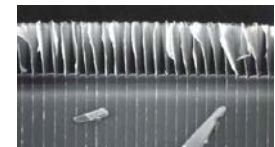
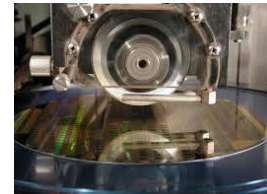
High Temperature DC-Bus Capacitors Cost Reduction and Performance Improvements

- Delphi-provided material properties and capacitor construction details are being interpreted
- ORNL shall inform Delphi of what additional properties will be needed for the thermal analysis and thermo-mechanical analysis of the capacitor.
 - Many of those properties were generated using dynamic methods
 - Representativeness of such data for a material can be compromised if that material is non-linear and subjected to relatively large amounts of strain
- A finite element model geometry of the capacitor is under construction at ORNL
 - Simplifications are under consideration that will reduce computational solution time without compromise to accuracy and validity of results
 - The model will be sufficiently generic to accommodate new and future inputs for the various involved properties and geometries
 - ANSYS, and its pre-processing CAD software, DesignModeler, are being used

Technical Accomplishments – Pilot Line Upgrades

High Temperature DC-Bus Capacitors Cost Reduction and Performance Improvements

- **Monomer Delivery System**
 - A closed-loop PID control system has been designed to accurately feed liquid monomer into the flash evaporator. This includes a precision pumping and monomer flow metering system.
- **Upgrade to a Higher Capacity Flash Evaporator**
 - System already in place
- **Cutting of Mother Capacitor Material**
 - Precision dicing saw will be added to current manual dicing saw, capable of dicing 12"x12" mother capacitor plates into individual capacitors of different length and width
- **Plasma Ashing**
 - Large scale plasma ashing system will be added capable of handling PML DC-link capacitors as specified by Delphi
- **Arc Spray System**
 - Arc spray system and hood will be sourced to eliminate reliance on third party system that is not specifically designed to terminate PML capacitors



Technical Accomplishments – Pilot Line Upgrades (cont'd)

High Temperature DC-Bus Capacitors Cost Reduction and Performance Improvements

- Other components of the Pilot Line Scale-up
 - In-chamber system to passivate the aluminum electrodes
 - Improvements to existing aluminum evaporation system
 - Mother capacitor heat setting system
 - Various fixtures designed to handle specific size PML capacitors through the various process steps
- All major pilot equipment will be in-house by the end of the 2Q and will be processing capacitors by the 3Q of 2014

Technical Accomplishments – Optimize PML Dielectric for Gen1 Capacitor

High Temperature DC-Bus Capacitors Cost Reduction and Performance Improvements

- The current pilot line is used to produce small size capacitors with an optimized polymer dielectric system and metallized electrodes
- Key variables taken into consideration when optimizing the polymer dielectric and capacitor electrodes include:
 - Breakdown strength
 - Self healing properties
 - Energy density
 - Mechanical properties as they impact capacitor processing and self-healing
 - Ease of flash evaporation
 - Capacitance stability with temperature up to 140°C
 - Dissipation Factor stability up to 140°C with an upper limit <0.01

Technical Accomplishments – Optimize PML Dielectric for Gen1 Capacitor (cont'd)

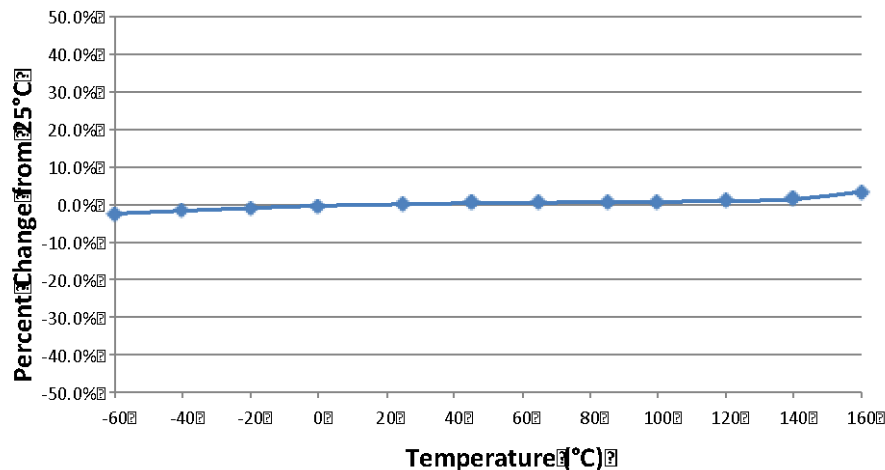
High Temperature DC-Bus Capacitors Cost Reduction and Performance Improvements

Dielectric A:

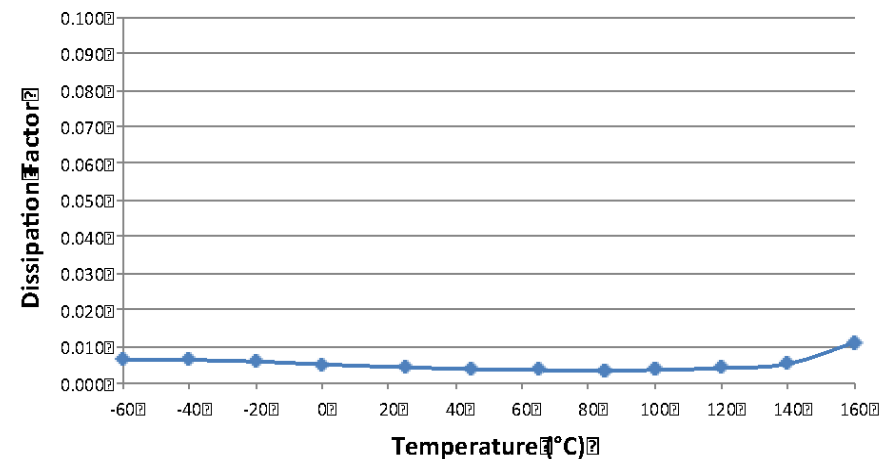
Small-area PML capacitor with 2000 layers

Dielectric Thickness 0.90 μm , Capacitance 25 μF , Dielectric Constant 3.0

Change in Capacitance



Dissipation Factor



T_g close to 160°C = Stable dielectric up to about 140°C

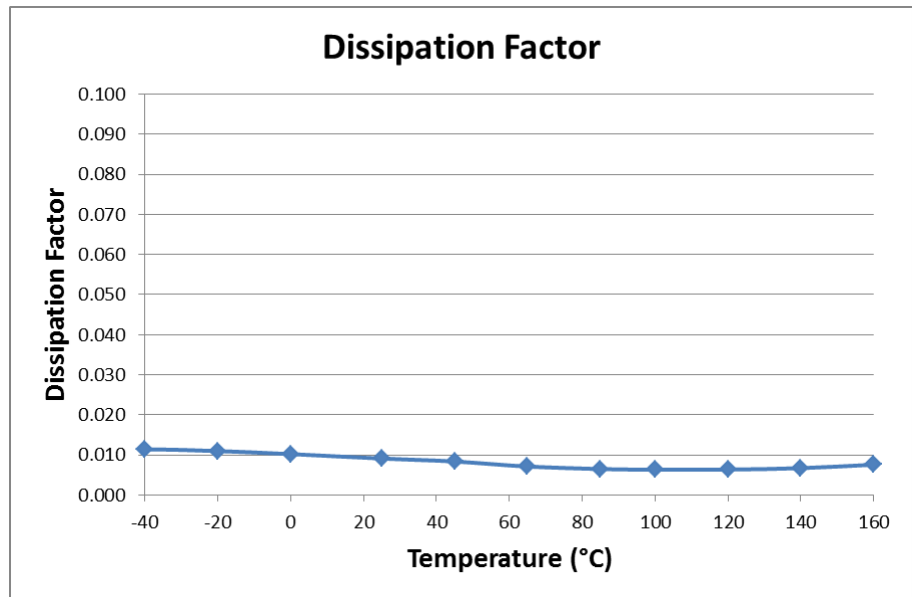
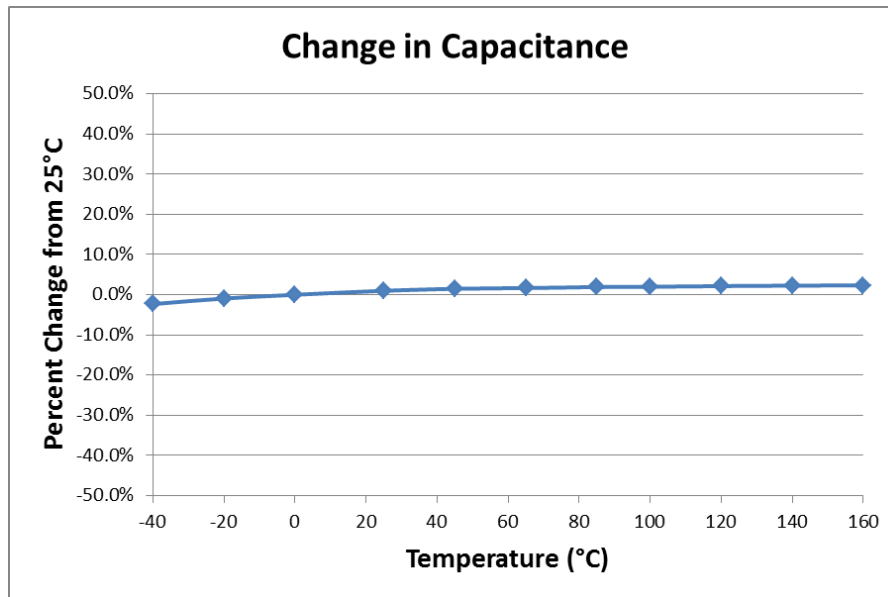
Technical Accomplishments – Optimize PML Dielectric for Gen1 Capacitor (cont'd)

High Temperature DC-Bus Capacitors Cost Reduction and Performance Improvements

Dielectric B:

Small-area PML capacitor with 1000 layers

Dielectric Thickness 0.84 μm , Capacitance 14 μF , Dielectric Constant 3.2



$T_g > 160^\circ\text{C}$ = Stable dielectric at temperature $> 160^\circ\text{C}$

Collaboration / Coordination with Other Institutions

High Temperature DC-Bus Capacitors Cost Reduction and Performance Improvements

- Delphi Automotive Systems, LLC
 - U.S.-based Tier 1 supplier to many U.S. and non-U.S. automotive OEMs
 - Delphi has been actively developing inverters and other power electronics products, including battery energy storage systems, for these OEM customers for over 30 years
- Oak Ridge National Laboratory
 - Power Electronics and Electric Machinery Research Center (PEEMRC) is the U.S. Department of Energy's (DOE) premiere broad-based research center for power electronics and electric machinery development
 - The PEEPSRC facilities include state-of-the-art laboratory equipment, and the engineers are versant in a multitude of component and system level modeling programs

Remaining Challenges and Barriers

High Temperature DC-Bus Capacitors Cost Reduction and Performance Improvements

Phase I

- Will the pilot line upgrade be completed on time to produce and evaluate the performance of 800 μF / 400V / 600V_{transient} DC-link capacitors
 - Although there was some delay in the project starting date, the upgrade of the pilot line is on schedule
- Can PML Gen1 capacitors meet the projected improvements in thermomechanical performance and energy density?
 - Preliminary data suggests that PML capacitors will achieve and probably exceed the proposed performance targets

Phase II

- Can PML Gen2 capacitors pass the stringent AEC-Q200 Rev D Test Plan?
 - Like all metallized capacitors an effective package will be required to protect the aluminum electrodes from exposure to humidity at high temperatures

Future Work

High Temperature DC-Bus Capacitors Cost Reduction and Performance Improvements

- Rest of FY14
 - Complete PML dielectric optimization
 - Complete pilot line installation
 - Produce and evaluate Gen1 capacitors
 - Develop prototype package
 - Preliminary cost and commercialization plan
- FY15
 - Complete package design and evaluate packaged Gen1 capacitors
 - Complete cost analysis and commercialization plan
 - Develop Gen2 capacitors
 - Package and evaluate Gen2 capacitors
 - Develop business plan
- FY16
 - Test packaged Gen2 PML DC-link capacitors according to AEC-Q200 Rev D Test Plan
 - Integrate and test Gen2 PML DC-link capacitors in a Delphi inverter
 - Pursue business plan for transition into production

Critical Assumptions and Issues

High Temperature DC-Bus Capacitors Cost Reduction and Performance Improvements

- PML capacitor dielectrics can withstand 140°C operating temperature
 - PML capacitor material is currently heat set at >220°C
 - Preliminary results on capacitance and dissipation factor as a function of temperature indicate stability up to at least 160°C
- As PML capacitors are significantly smaller than current PP capacitors, heat due to ESR and DF losses must be effectively dissipated to minimize the maximum capacitor temperature
 - Delphi and ORNL are developing a dynamic thermo-mechanical numerical model to optimize capacitor package, lead connections and physical location in the inverter to maximize heat dissipation
- PML Gen2 capacitors will pass the AEC-Q200 Rev D Test Plan
 - Low voltage surface mount, unpackaged, PML capacitors currently pass consumer electronic specific electrical and environmental tests. Based on this, there is a high probability that packaged PML Gen2 capacitors will pass the more stringent AEC-Q200 Rev D Test
- PML Gen2 capacitors will cost less than 50% of the of PP film capacitors
 - This assumption is based on the cost of acrylate monomers and the vertical integration of capacitor manufacture, which reduces cost and eliminates the profit margins of the film producers and metallizers. Also thinner dielectric and higher ϵ_r requires less time in process and materials.