Electro-thermal-mechanical Simulation and Reliability for Plug-in Vehicle Converters and Inverters

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Project ID # APE 026

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U.S. DEPARTMENT OF ENERGY
Energy Efficiency & Renewable Energy

Overview

USDRIVE
DRIVING RESEARCH AND INNOVATION FOR VEHICLE EFFICIENCY AND ENERGY SUSTAINABILITY

Work Timeline

- June 2011
- June 2014
- 90% Complete

Budget

- **Total project funding**
  - $700K
- **Funding received in FY11**
  - $ 200K
- **Funding received in FY12**
  - $ 300K
- **Funding received in FY13**
  - $ 200K

Barriers

Need electro-thermal-mechanical modeling, characterization, and simulation of advanced technologies to:

- **Improve electrical efficiency**
- **Improve package thermal performance and increase reliability**
- **Reduce converter cost**

Partners

- NIST- Electro-thermal modeling
- UMD/CALCE – Reliability modeling
- VTech – Soft switching module
- Delphi – High current density module
- Powerex – Module technology
- NREL – Cooling technology

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Goal: Electro-Thermal-Mechanical Simulation

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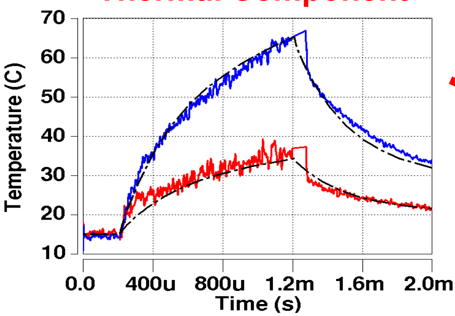
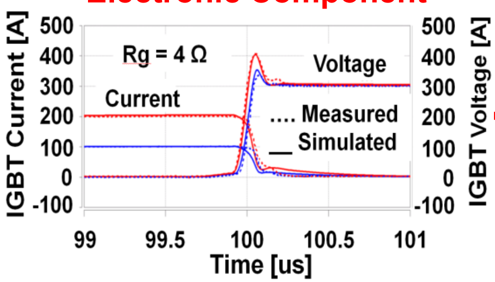
Models, Parameter Determination

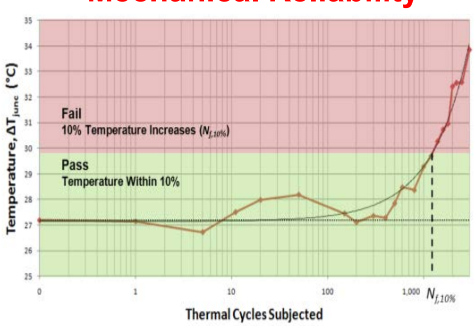
Thermal Component



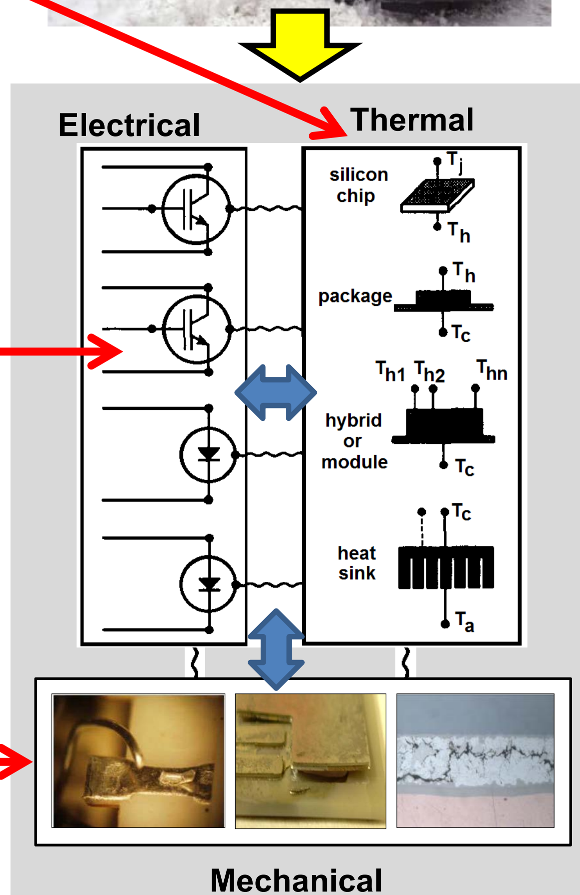
Electronic Component



Mechanical Reliability

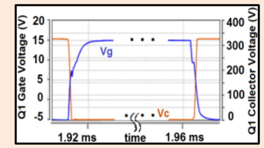


Driving Cycles, Environmental Conditions



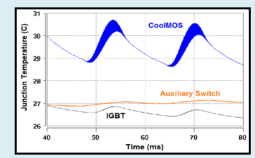
Simulation Applications

Electrical



- Inverter performance evaluation
- Advanced topology design
- Advanced device integration

Electro-Thermal



- Electro-thermal interactions,
- SOA and failure mechanisms,
- Cooling system impacts.

Reliability

- Reliable integration of advanced technologies
- System reliability evaluation.
- In-Vehicle applications:
  - Maintaining component health,
  - Predicting service needs,
  - Operation with partially degraded capacity near component end-of-life.

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Relevance

Objective:

Provide theoretical foundation, measurement methods, data, and simulation models necessary to optimize power module electrical, thermal, and reliability performance for Plug-in Vehicle inverters and converters.

FY13 - FY14 Goals:

1) Analyze **Viper SOA** using dynamic electro-thermal simulation with models including high voltage, high current parameter extraction
2) Develop **Cross-Coupling TSP Measurement** capability and use to validate thermal coupling model within VTech module thermal model
3) Develop **Thermal Component Models for Air and Liquid-Cooled Heatsinks** and include in electro-thermal simulation of Viper and VTech modules
4) Perform thermal cycle measurements to **extract parameters for Physics-of-Failure Models** and use in electro-thermal-mechanical simulation
5) Develop **electro-thermal models for advanced semiconductor devices** e.g., SiC MOSFETs and SiC JFETs and GaN diodes
6) **Evaluate the impact of advanced technologies** such as wide bandgap semiconductors and advanced power module package technology

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FY13-14 Milestones/Decision Points

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Month/Yr	Milestone
Aug. 12 (complete)	1) Used electro-thermal-mechanical simulations to validate measurement during fault conditions and evaluated thermal stresses in Viper module.
July 13 terminated	2) Incorporate Failure Models into Electro-Thermal Simulation using results of thermal cycling degradation and monitoring measurements on two DBC stacks.
Sept. 12 (complete)	3) Developed thermal-network-component models for representative cooling systems.
Oct. 12 (complete)	4a) Used simulations to evaluate thermal stresses at module interfaces for VTech module,
Oct. 12 terminated	4b) and use Physics-of-Failure Models to calculate damage and evaluate impact on VTech module
Jan. 13 terminated	4c) Calculate increase in thermal resistance at interfaces in VTech module due to thermal cycling damage and use changing resistance in the thermal network during simulations.
Mar. 13 (complete)	5) Included liquid- and air-cooling thermal network component models in electro-thermal simulations of vehicle inverters.
June. 13 (complete)	6) Developed electro-thermal models for advanced semiconductor devices including SiC MOSFETs, SiC JFETs and GaN diodes.
May. 14 (ongoing)	7) Include advanced Wide-Bandgap Semiconductor Device Models in simulations to optimize high current density, low thermal resistance, and soft-switching modules.
July 14	Investigate using NREL bonded interface reliability characterization

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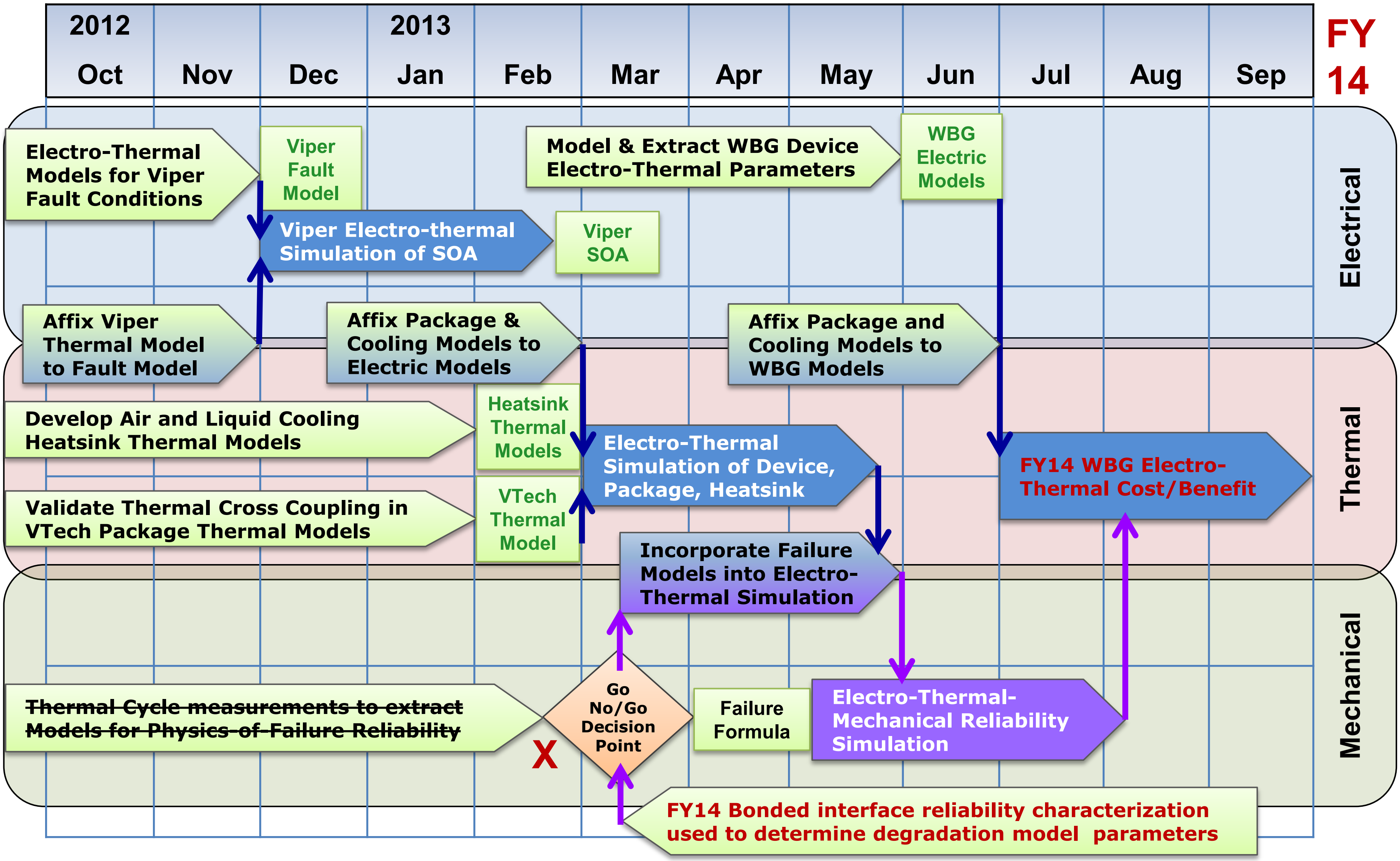
FY13-14 Tasks to Achieve Goals



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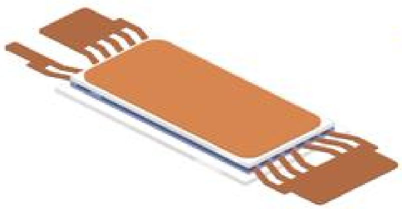
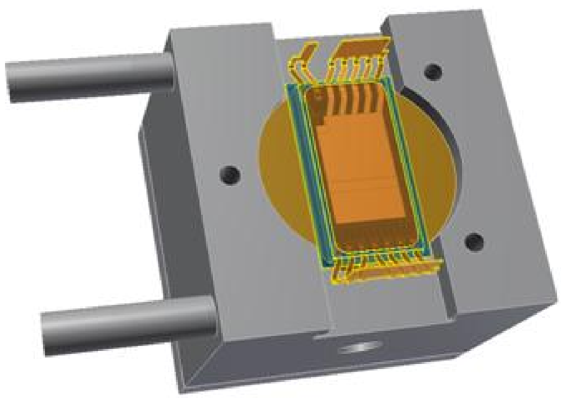
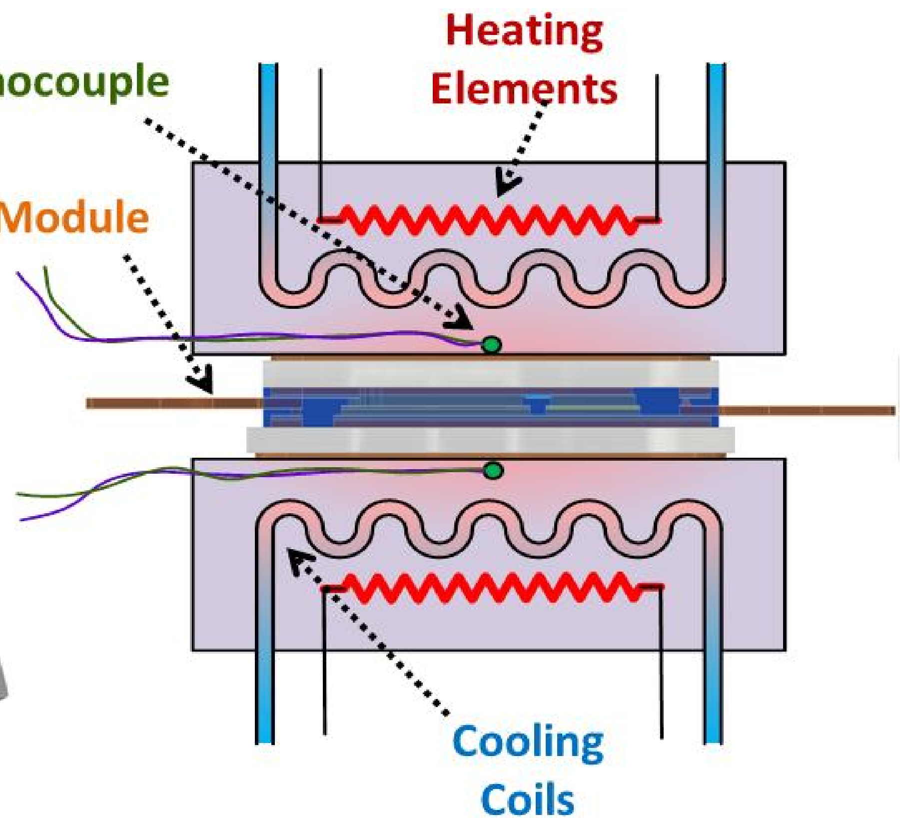
Approach/Methods: Measurement, Modeling, and Simulation

- **Developed dynamic electro-thermal Saber models, parameter extractions, and validation of models for:**
  - Silicon IGBTs and PiN Diodes
  - Silicon MOSFETs and CoolMOSFETs
  - SiC Junction Barrier Schottky (JBS) Diodes
  - SiC MOSFETs
- **Developed thermal network component models and validated models using Transient Thermal Imaging (TTI) and high-speed Temperature Sensitive Parameter (TSP) measurement:**
  - Power Semiconductor Chip
  - Package: Delphi VIPER and VTech Soft Switching modules
  - Air and liquid cooling heatsinks
- **Developing thermal-mechanical degradation models and extract model parameters using accelerated stress and monitoring:**
  - Stress types include thermal cycling, thermal shock, power cycling
  - Degradation monitoring includes TTI, TSP, X-Ray, C-SAM, etc.
  - Investigate using NREL bonded interface reliability characterization

Application: Delphi Viper Module Double-Sided Cooling Model

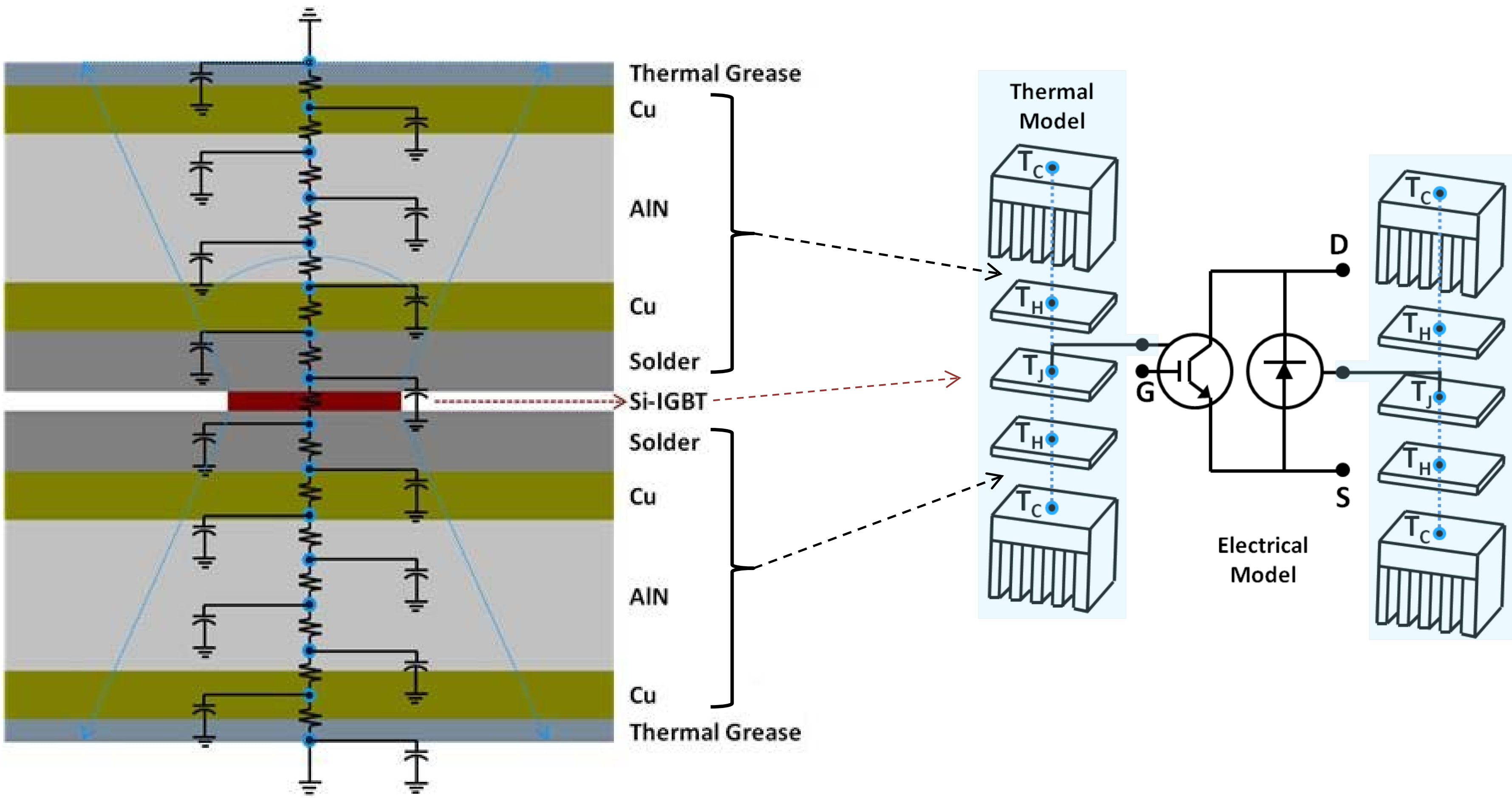




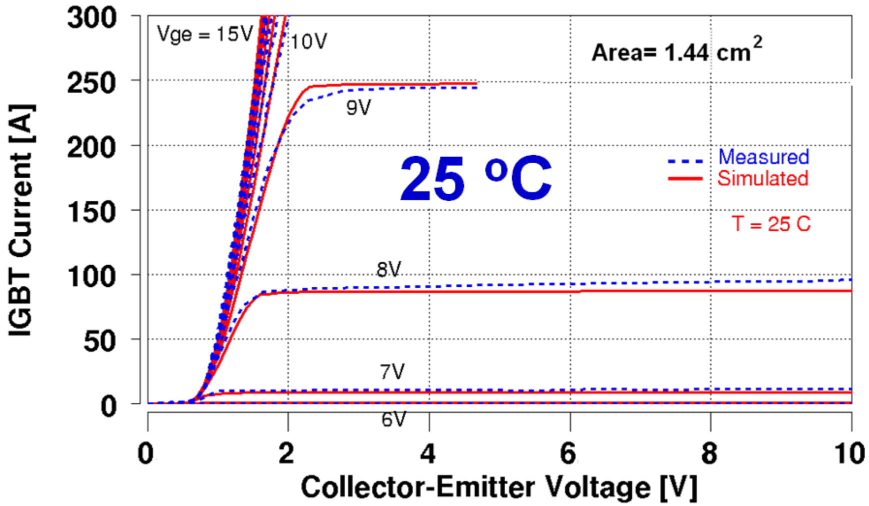


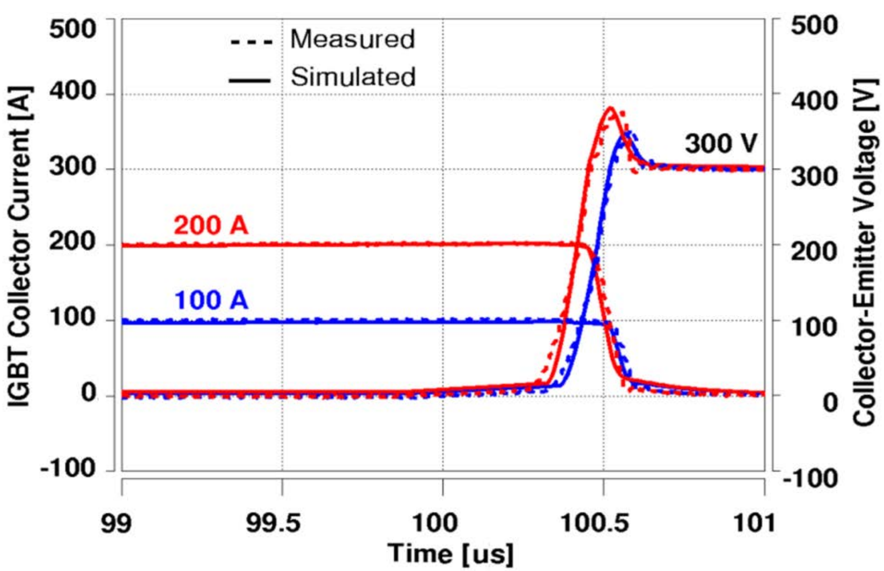
A doubled-sided temperature-controlled heatsink that was developed for the Viper module. This heatsink uses a spring-loaded piston to apply a controlled four kg compressional pressure to the device.

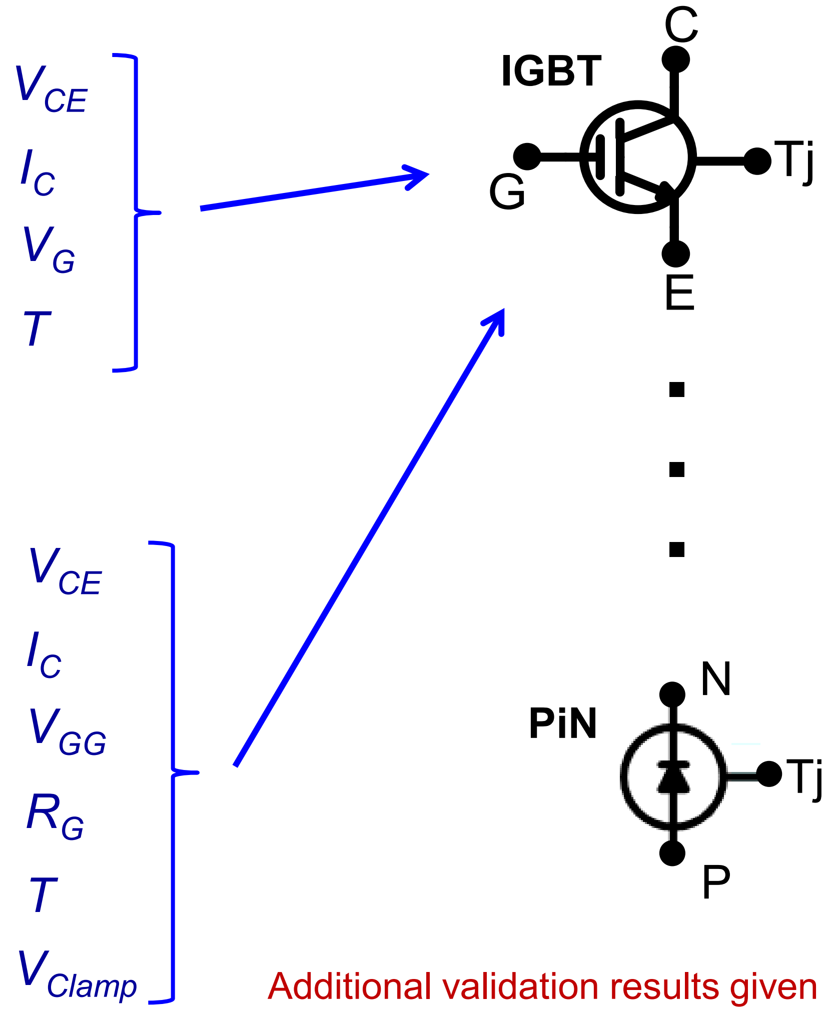
Method: Electro-Thermal Model for Double-Sided Cooling Viper Module



Parameter Extraction: Delphi-Viper Electro-thermal Semiconductor Models







Additional validation results given at FY12 PEEM Kickoff, FY 13 Merit Review, and FY13 Tech Team.

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Validation: Thermal Test Fixture Model

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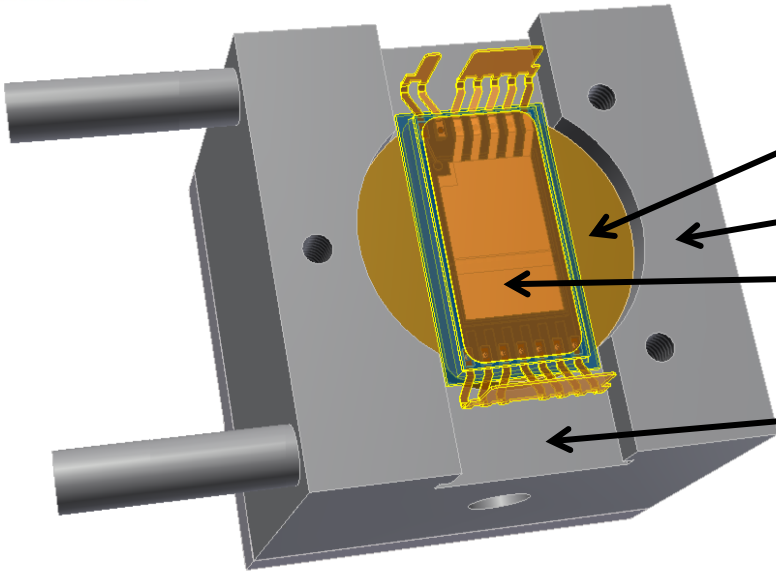
Viper module thermal test fixture



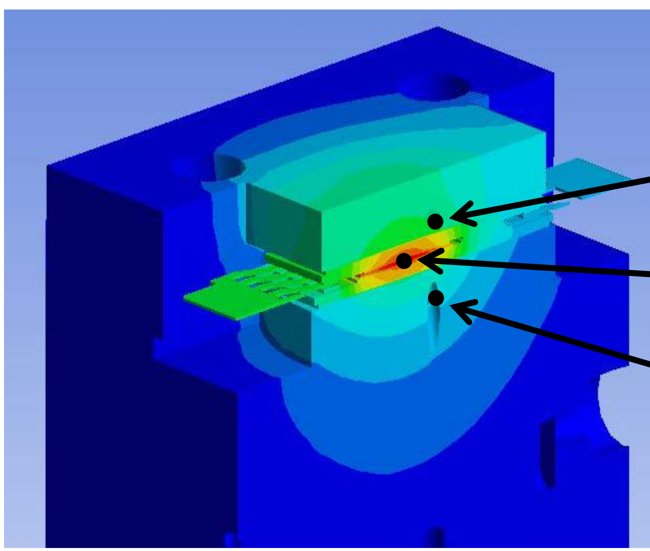
Piston

Top Cooling Plate (not shown)

Viper Module

Water Cooling Fixture

Viper module 262 W steady state ANSYS simulation for double-cooled test fixture



Top Plate Temperature (0.05” from edge)
37 °C (ANSYS model)
40.4 °C (Measurement)

Device Temperature
69 °C (ANSYS model)

Piston Temperatures (0.05” from edge)
28 °C (ANSYS model)
31.7 °C (Measurement)

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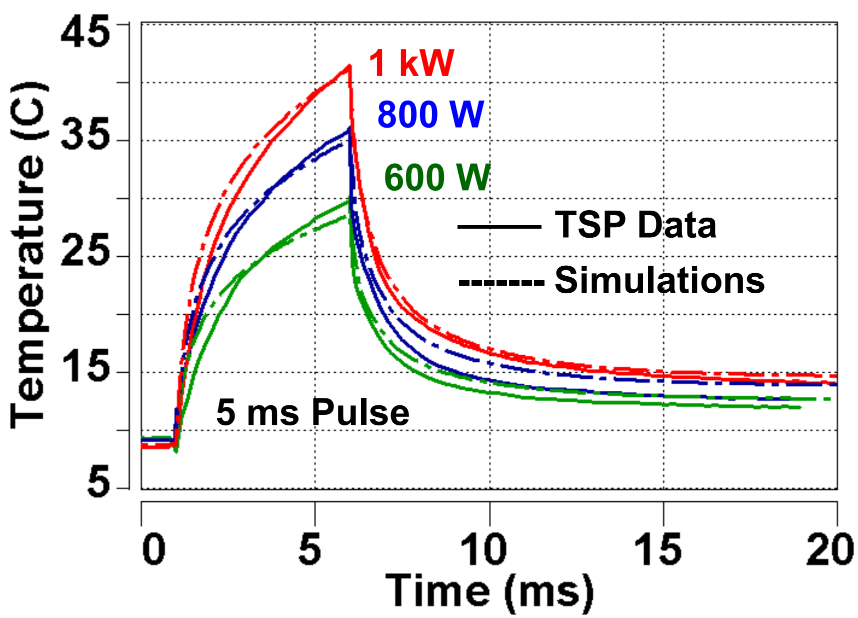
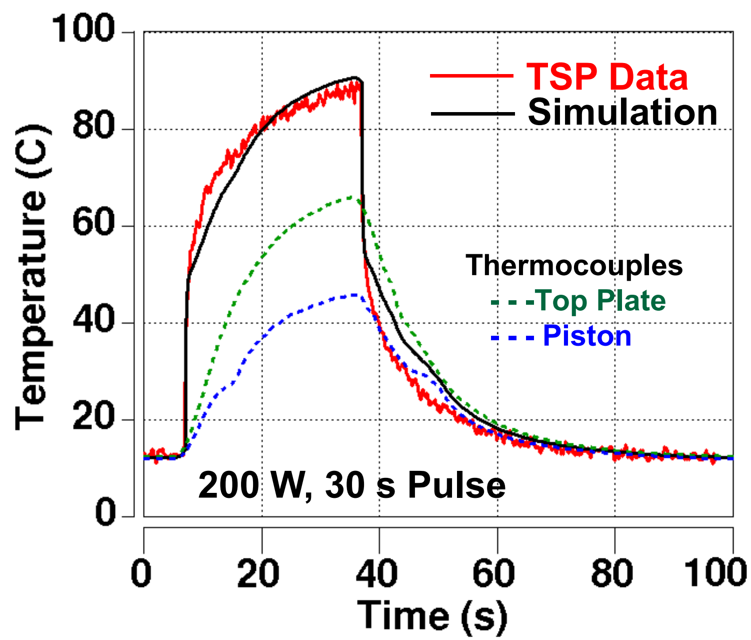
Validation: Thermal Network Component Model for Viper Module Package

- Test fixture used to validate thermal model of Viper die, package, and interface to copper plates using TSP measurements.
- Test fixture modeled and compared with ANSYS and TSP.



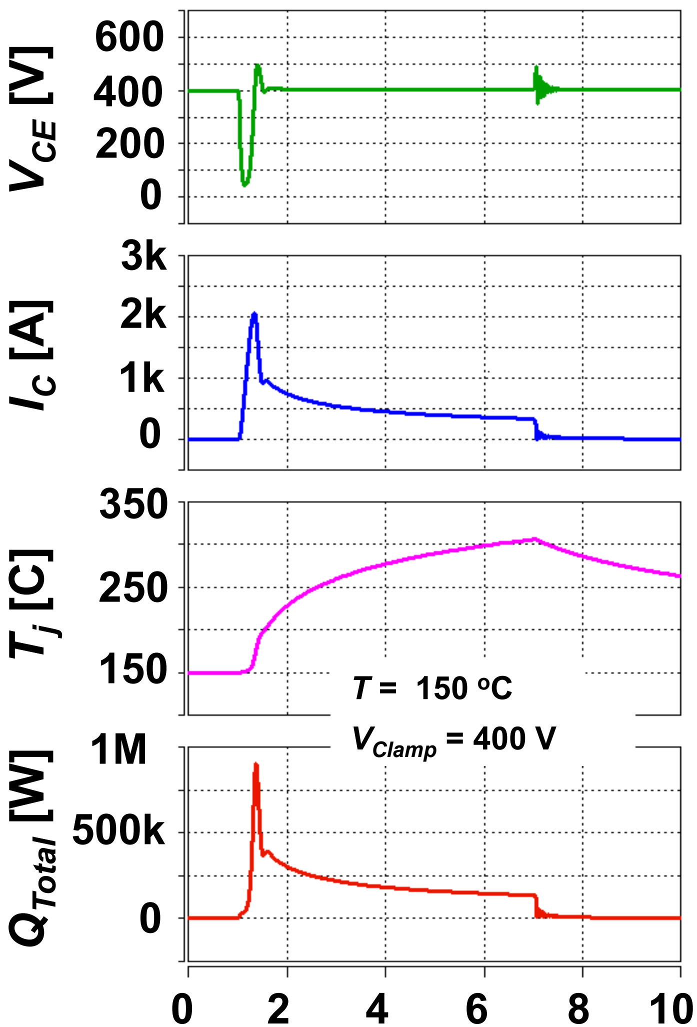
Comparison of simulated and measured Junction Temperature (TSP) for short duration, high power pulses.



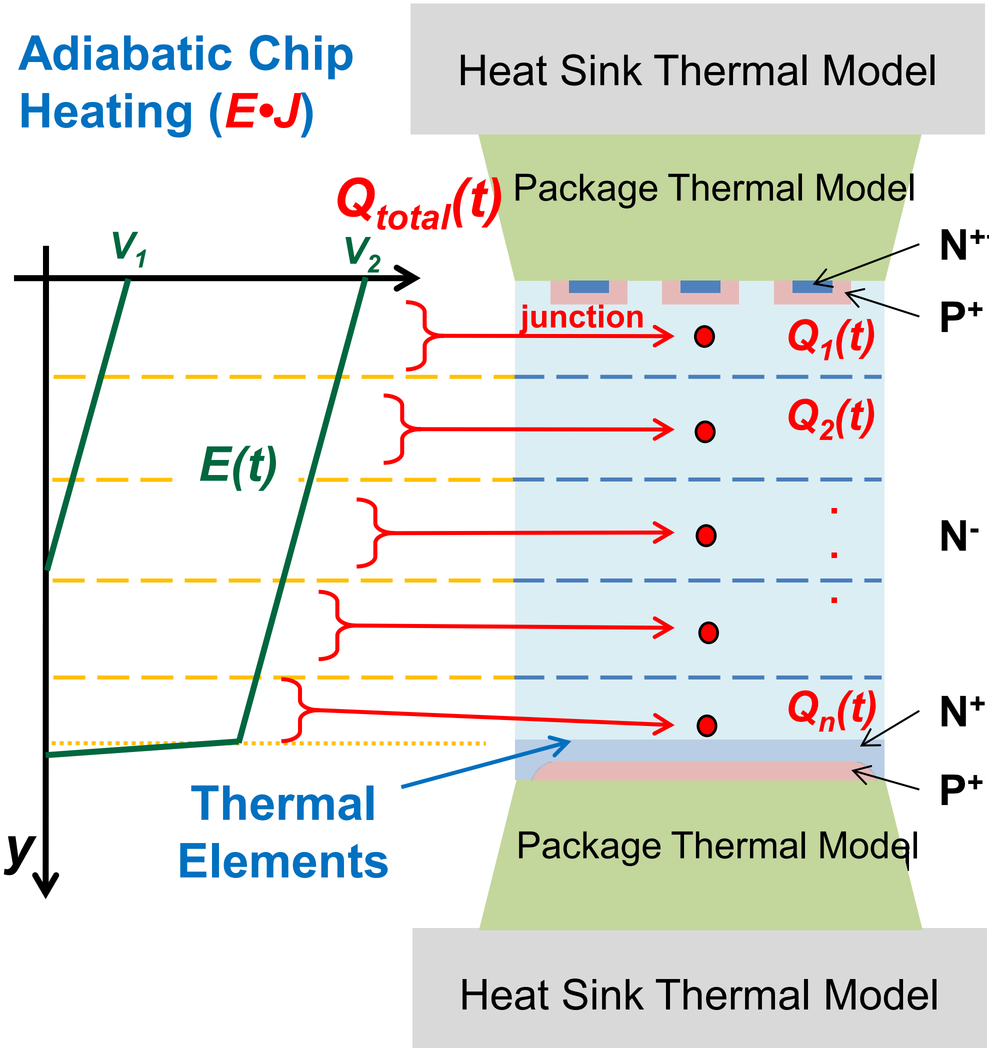
Comparison of simulated and measured Junction Temperature (TSP), and Plate and Piston Temperatures (thermocouples) for a low power, long duration pulse.

Method: Electro-Thermal Simulation Adiabatic Heating for Short Circuit Conditions

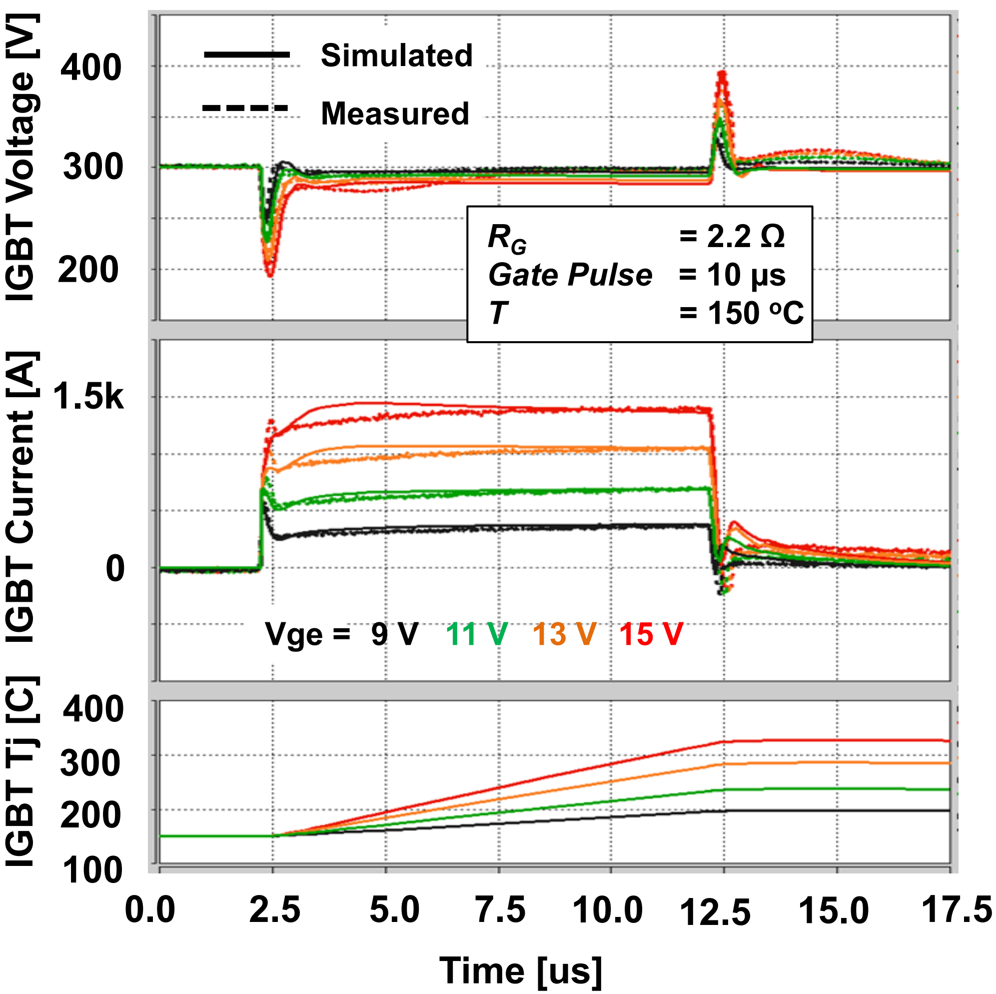
Short Circuit Simulation



Adiabatic Chip Heating (E•J)



Demonstration: Viper Module Simulation for Short Circuit Conditions



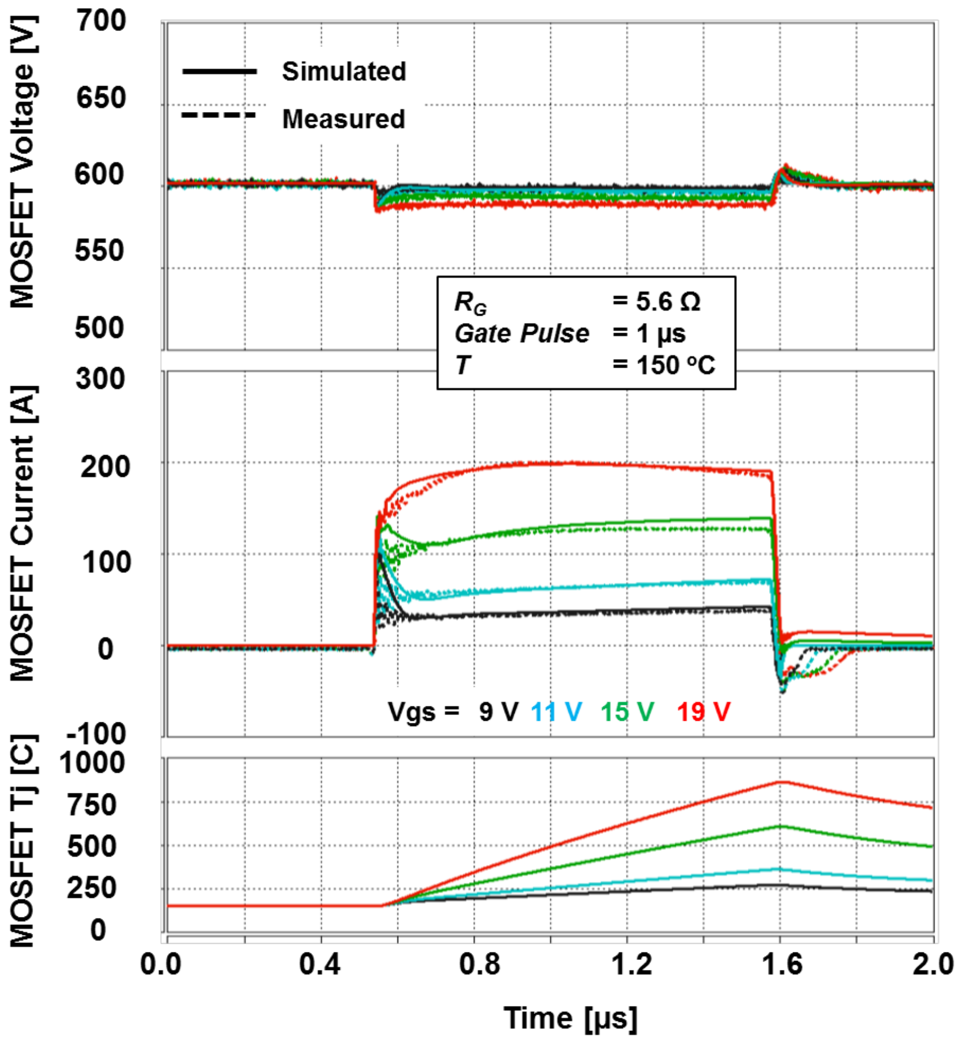
Required Tasks:

Extended and validated Viper IGBT model for high voltage, high current, high temperature conditions

- Narrow pulse width to reduce heating (3us)
  - Characterized test circuit: gate, collector and common emitter R & L
  - Varied Vgs, Rg, Vce, and T to characterize IGBT model
- Longer pulse width (10 us)
  - Current waveform validates thermal model for low Vg
  - High Vg extends IGBT model to high temperature

Then used simulations to analyze SOA performance

Demonstration: 1200 V, 30 A SiC MOSFET Simulation for Short Circuit Conditions



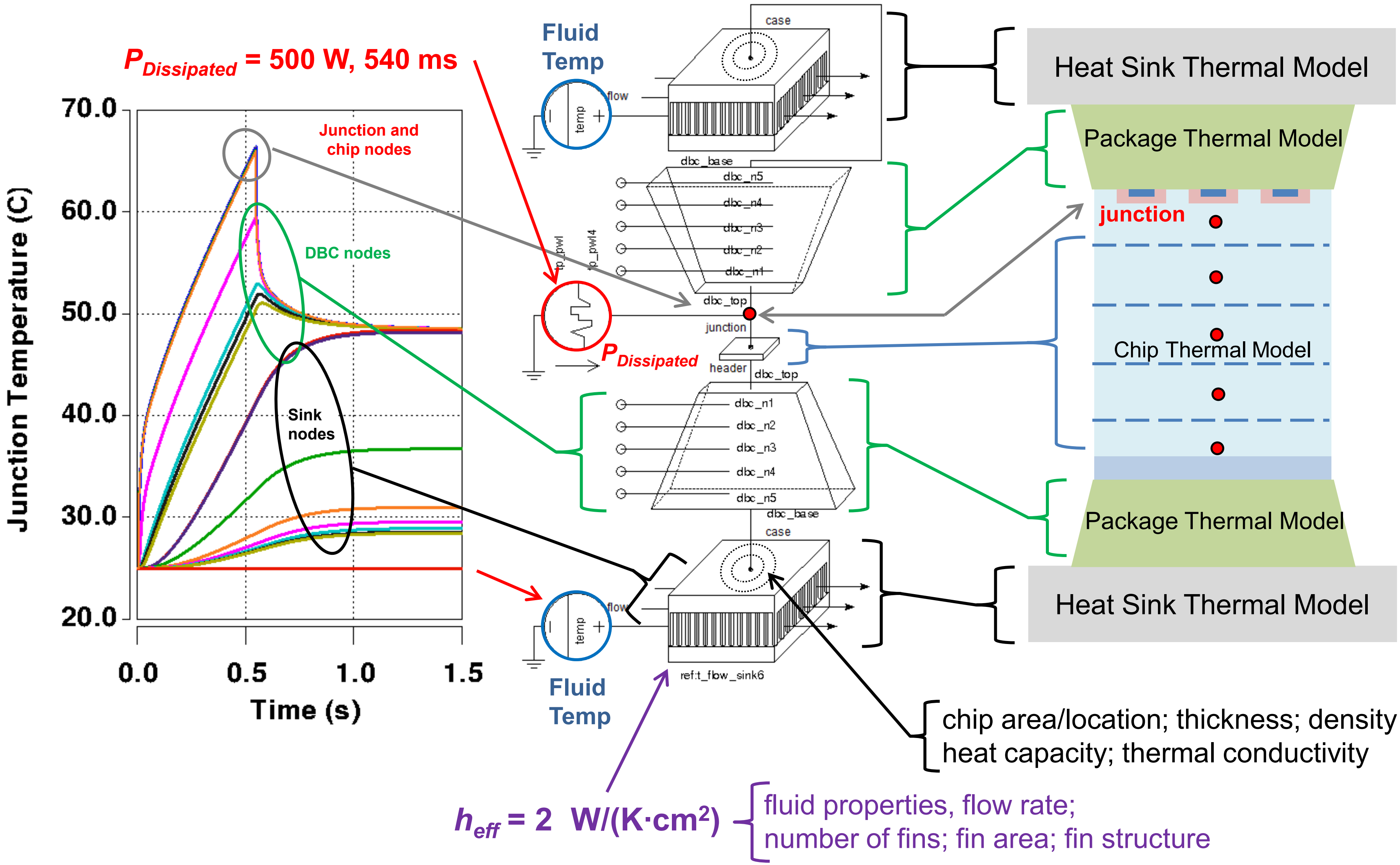
Required Tasks:

Extended and validated 1200 V SiC MOSFET model for high voltage, high current, high temperature conditions

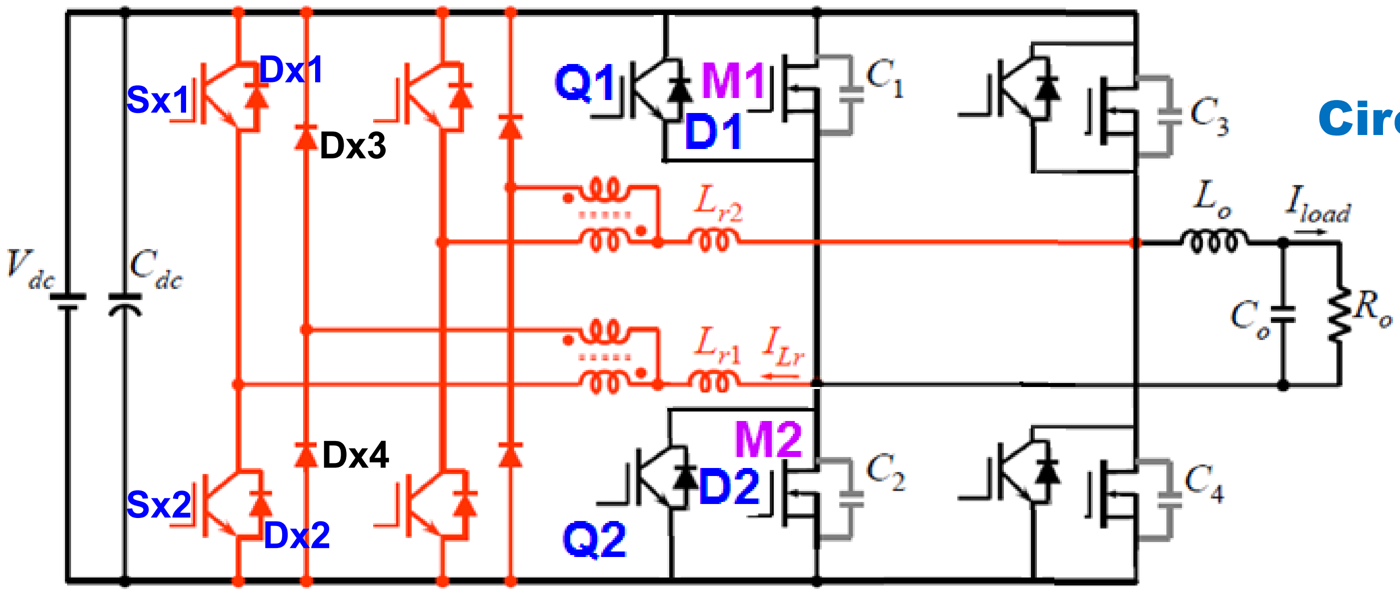
- Narrow pulse width to reduce heating (1us)
  - Characterized test circuit: gate, drain and source R & L
  - Varied Vgs, Rg, Vds, and T to characterize MOSFET model
- Updated MOSFET transconductance model for high temp SiC physics

Determined that SiC Power MOSFET has very high internal temperature after 1us short pulse at Vg=20 V, Vds=600 V due to thin voltage blocking layer

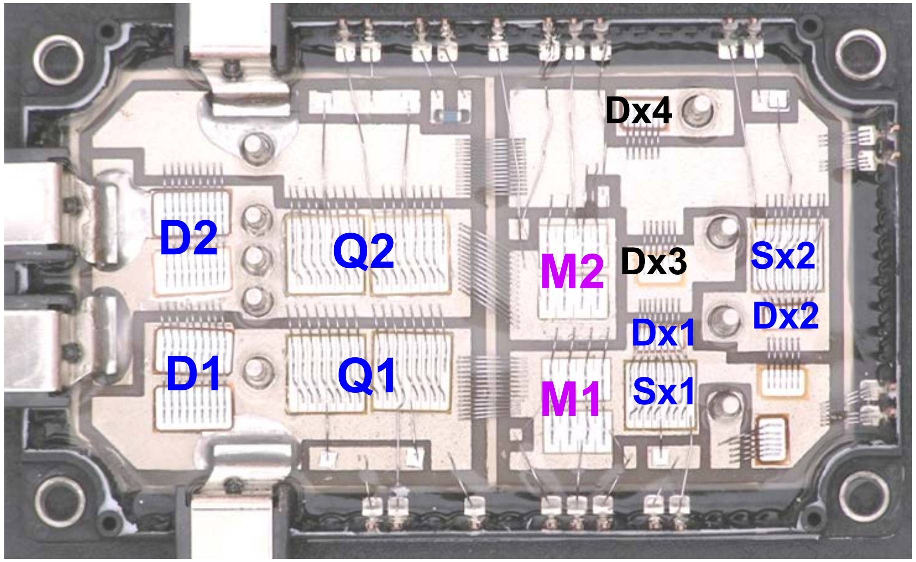
Demonstration: Liquid-Cooled Heatsink Viper Module Thermal Simulation



Application: VTech Soft Switching Module

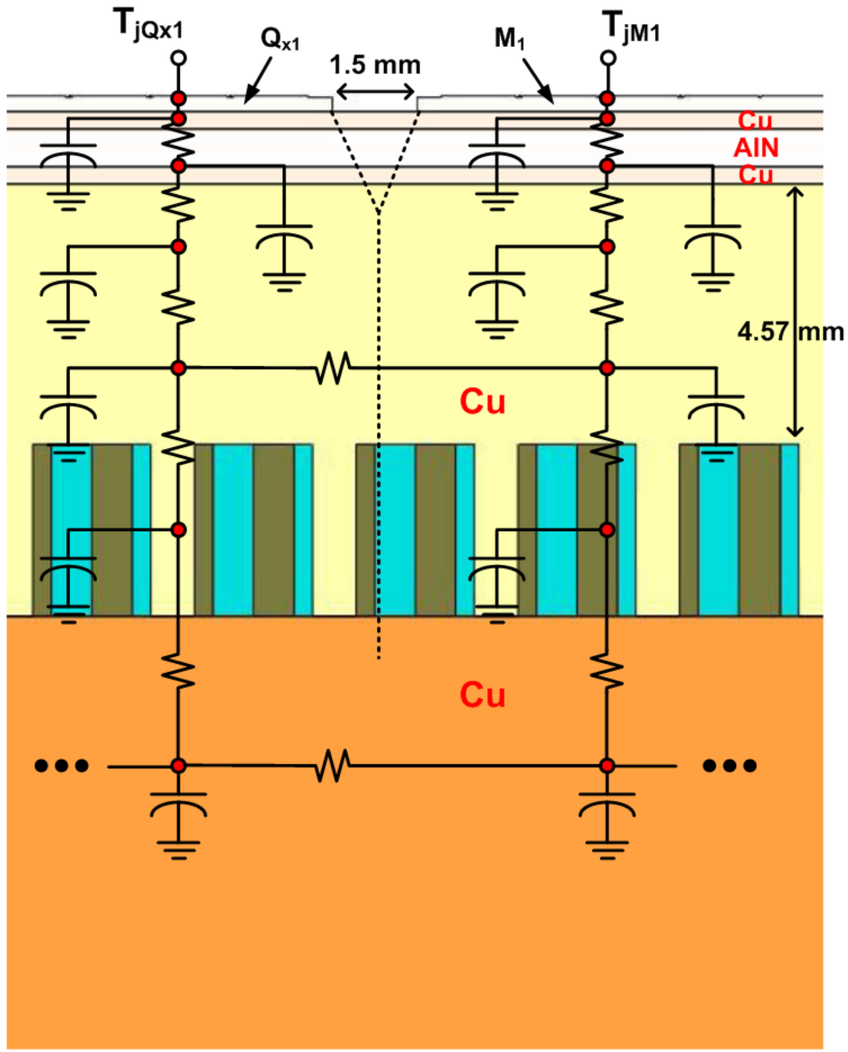


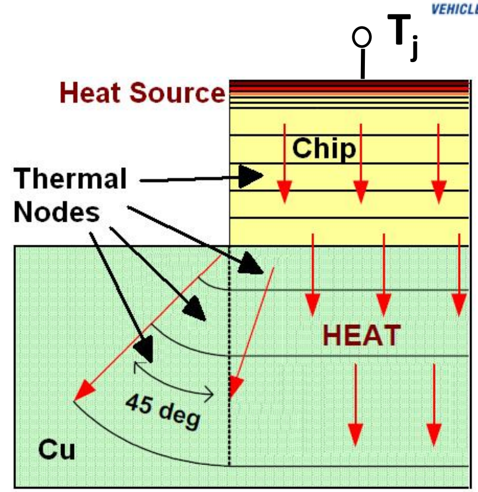
Circuit Diagram

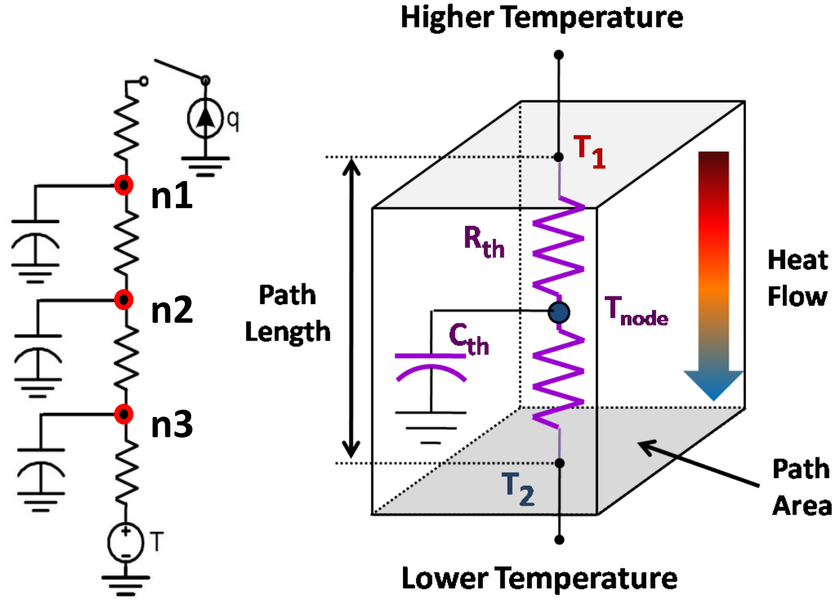


Module Components

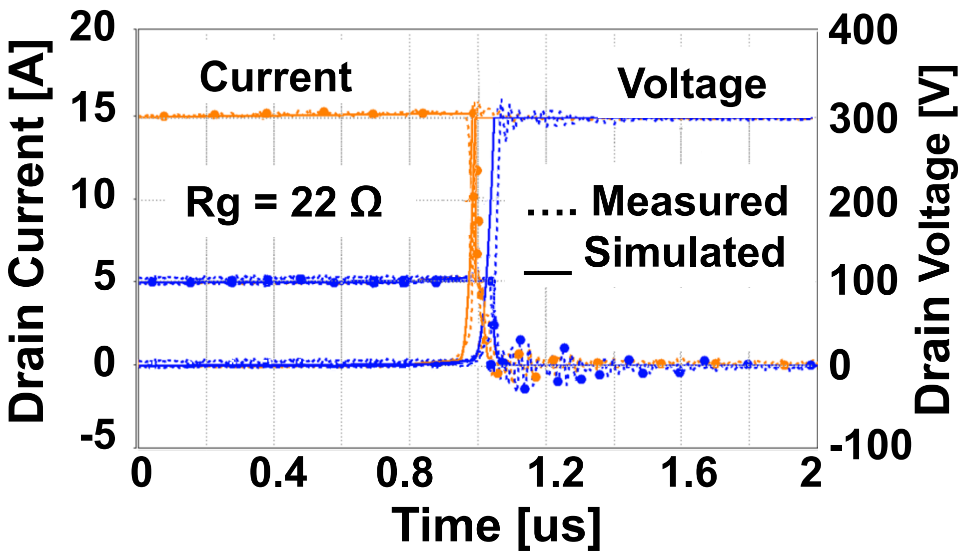
Method: Thermal Network Component Models

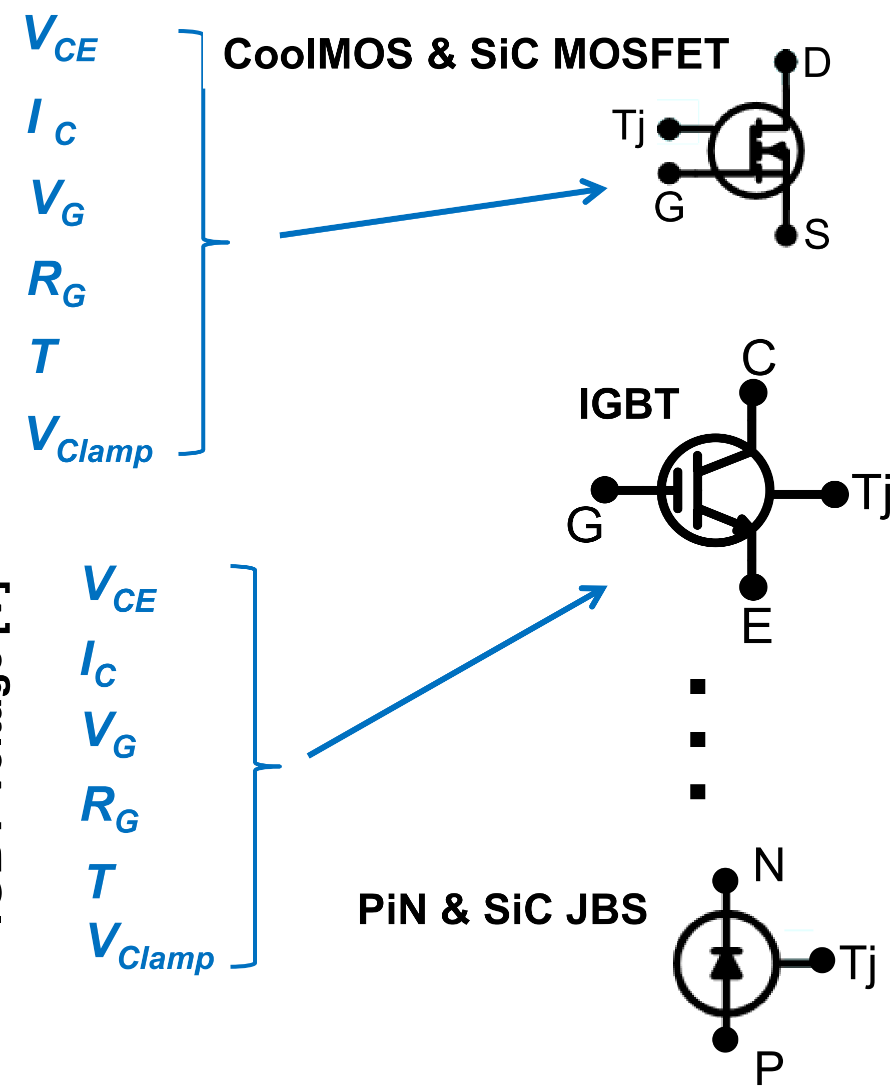


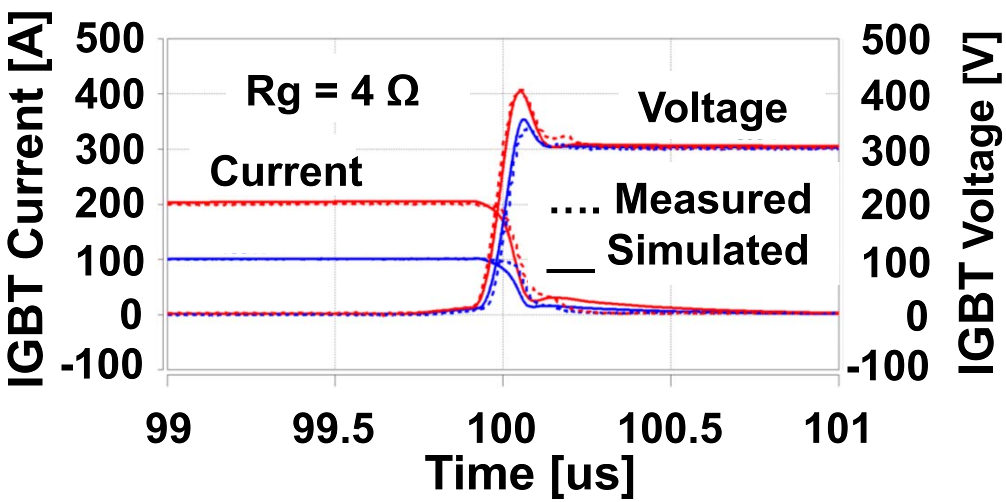




Parameter Extraction: Vtech Module, SiC devices
Electro-thermal Semiconductor Models



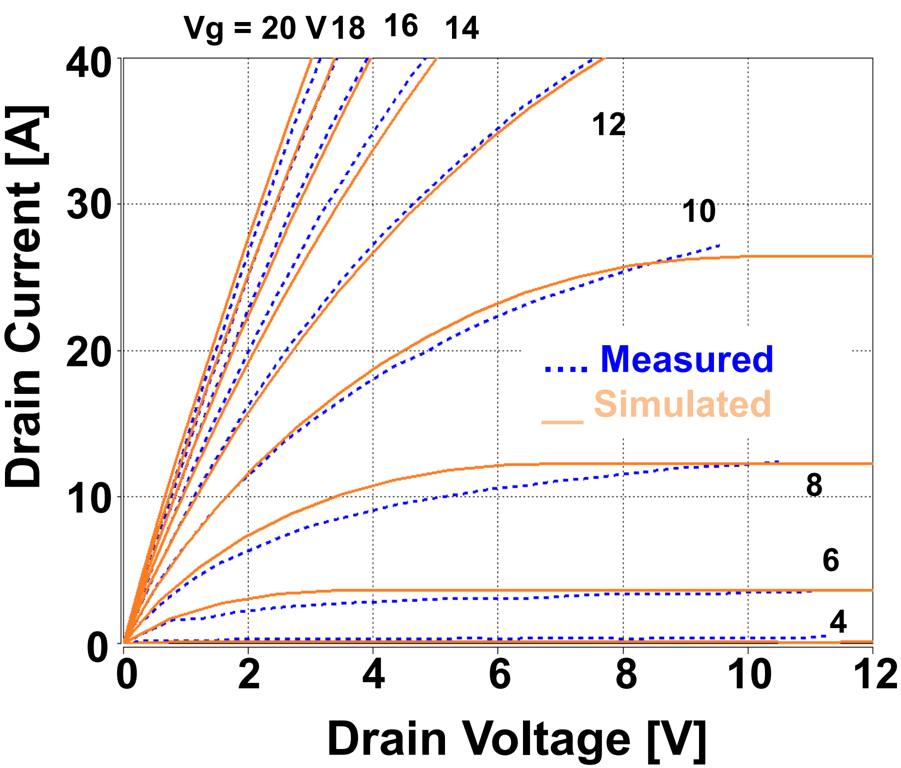




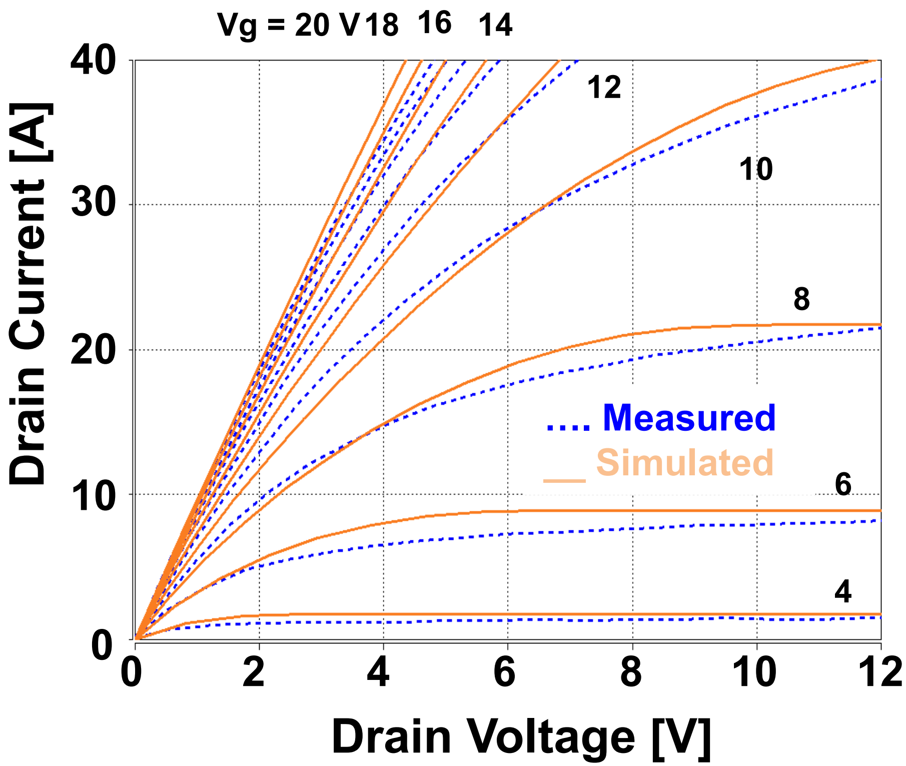
Additional validation results given at FY12 PEEM Kickoff, FY 13 Merit Review, and FY13 Tech Team.

Validation: 1200 V, 30 A SiC MOSFET Output Characteristics

25 °C

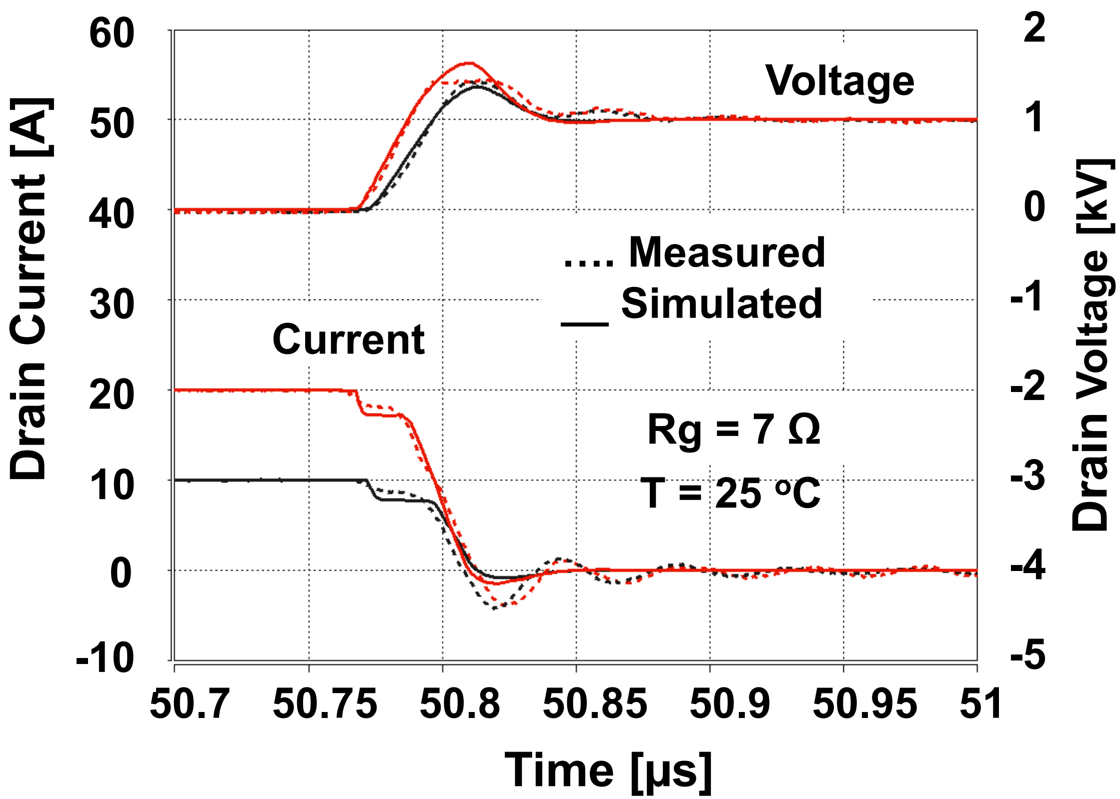


125 °C



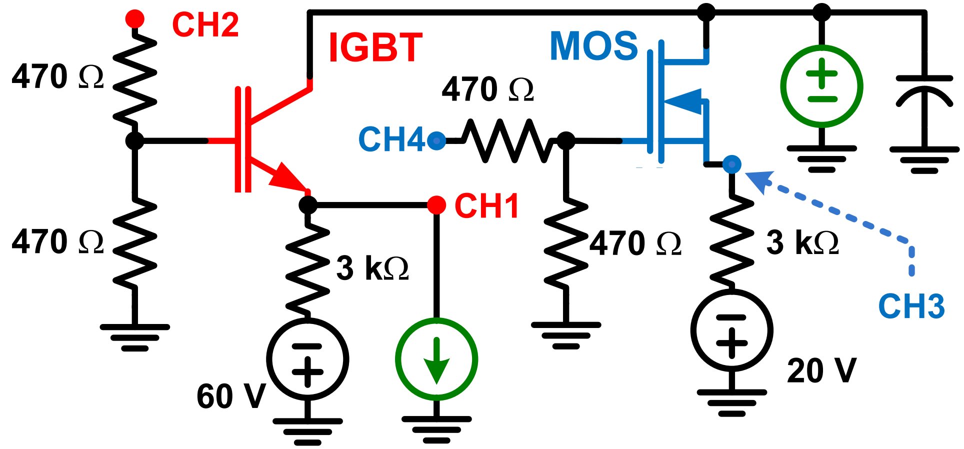
Validation: 1200 V, 30 A SiC MOSFET Inductive Load Turn-off

Current Dependence



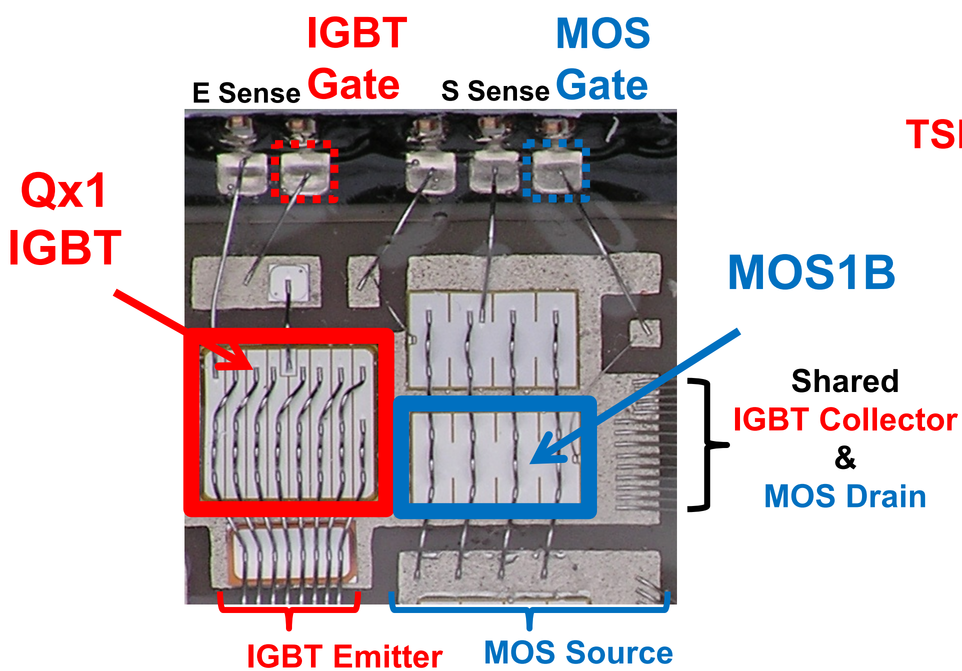
Method: Cross-Coupling TSP Measurement For VTech Module Paralleled IGBT/MOSFET

For the method to work, the **IGBT** has to dissipate a given **power** while the **MOSFET** remains off, and their gates must be measured independently.



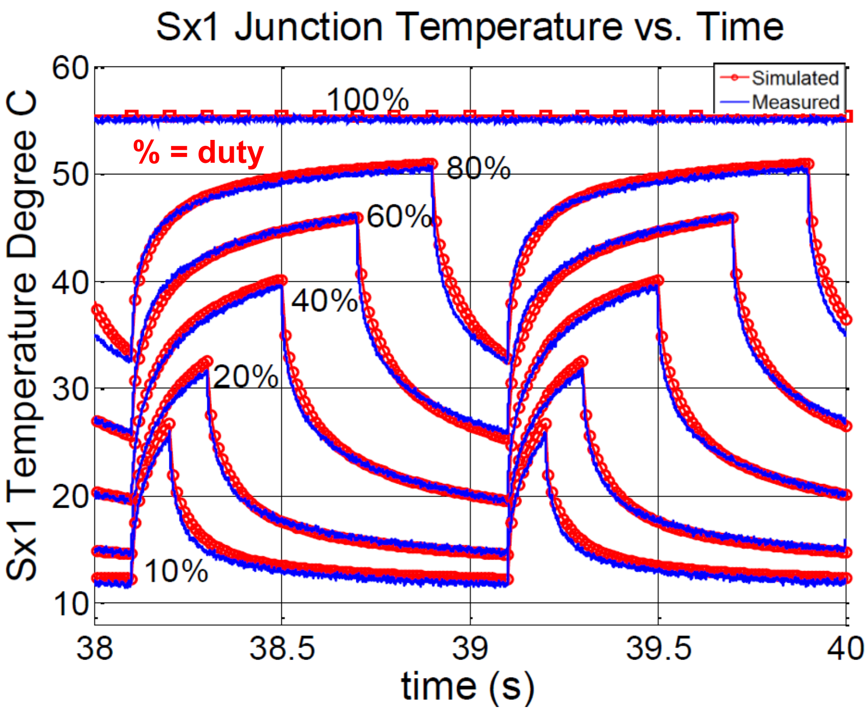
$TSP_{IGBT} = V_{CH1} - V_{CH2}$

$TSP_{MOS} = V_{CH3} - V_{CH4}$



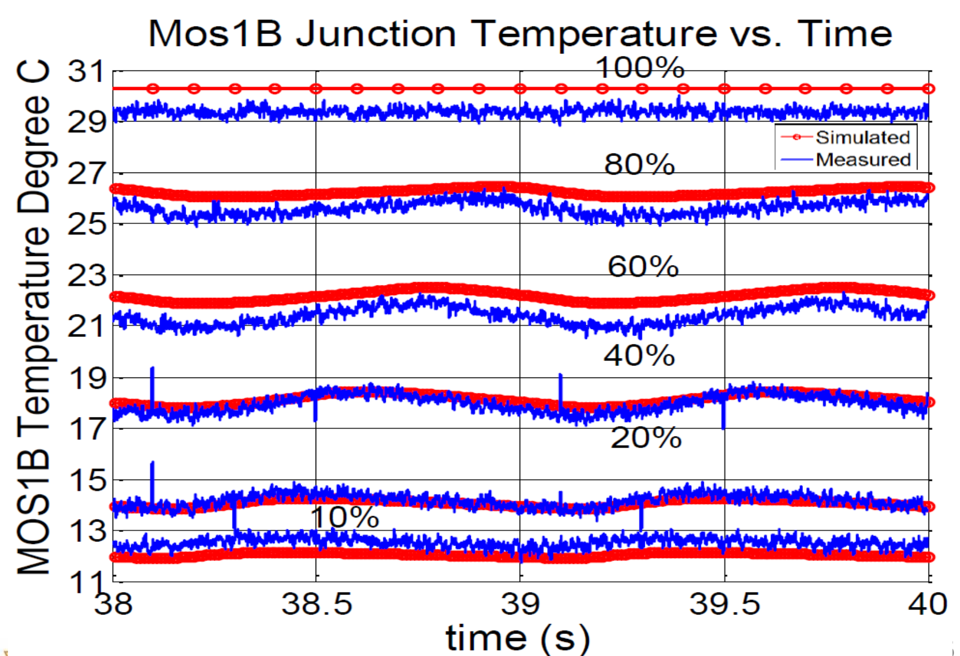
The devices were chosen for having physical proximity, different power dissipation ratings, and being thermally coupled through the same conductive layer on top of the DBC

Validation: Cross-Coupling TSP Measurement VTech Module Thermal Coupling Model



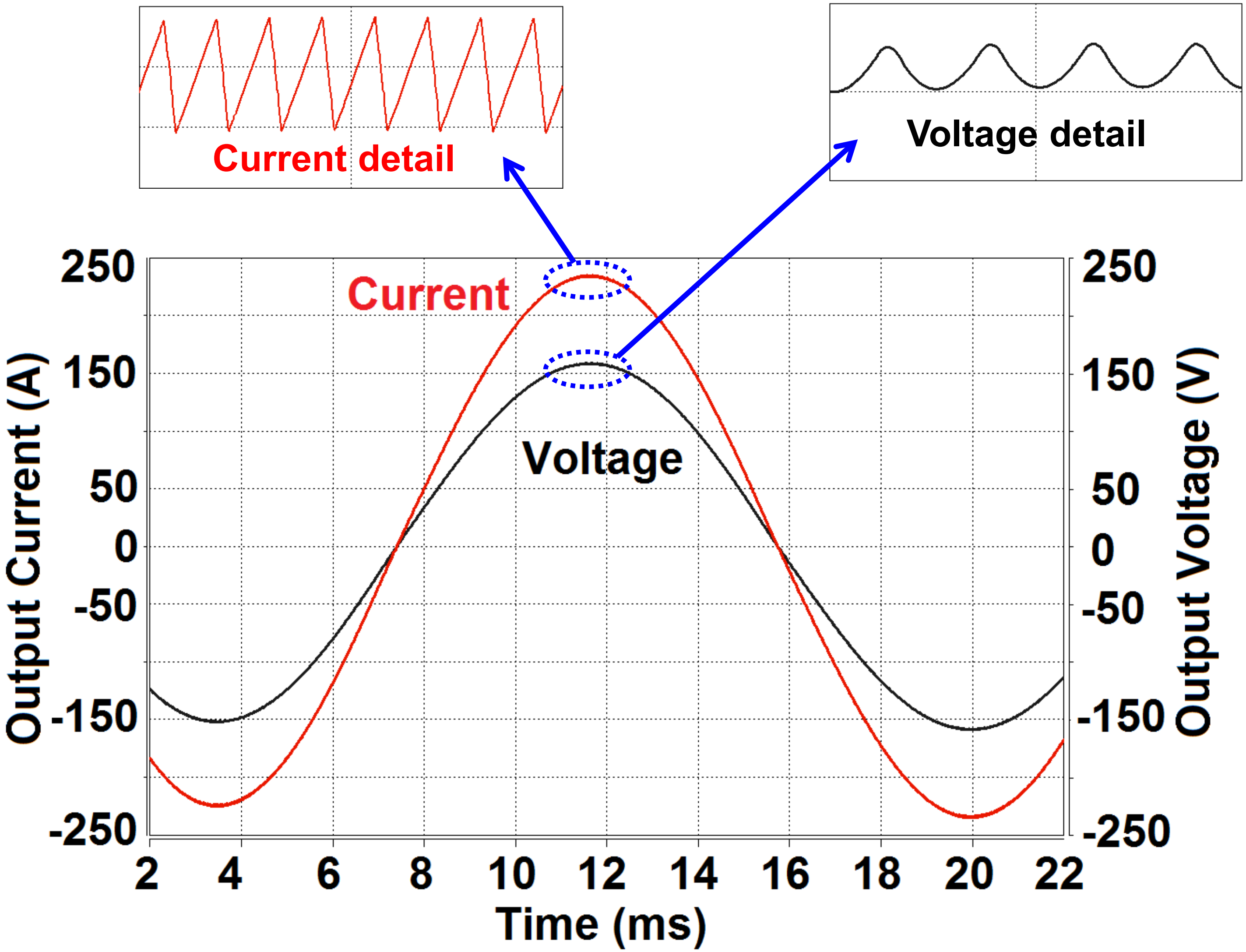
The IGBT was powered with a train of pulses at different duty cycles to generate enough average heat to be sensed in the MOS vicinity. Its measurements were used to validate the thermal transient behavior for the thermal stack model.

The thermal coupling model between adjacent power devices was validated using the MOS measurements.



Preliminary electro-thermal coupling model results for the MOS measurements show a close correspondence in their behavior.

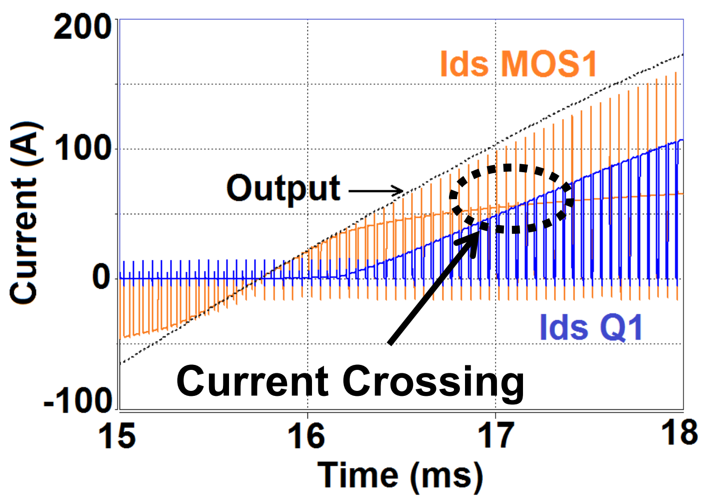
Analysis: Inverter Electro-thermal Simulation - VTech Module Electrical Waveforms

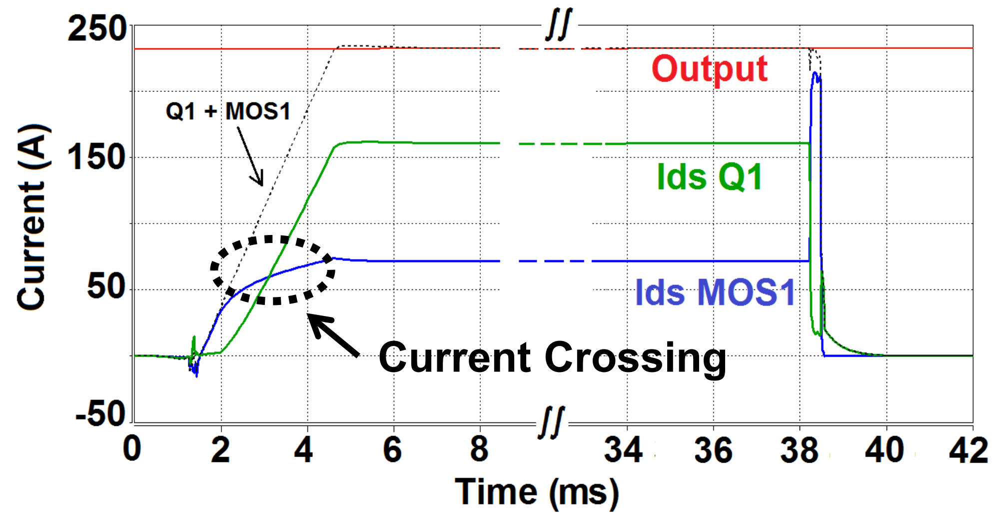


Inverter Output

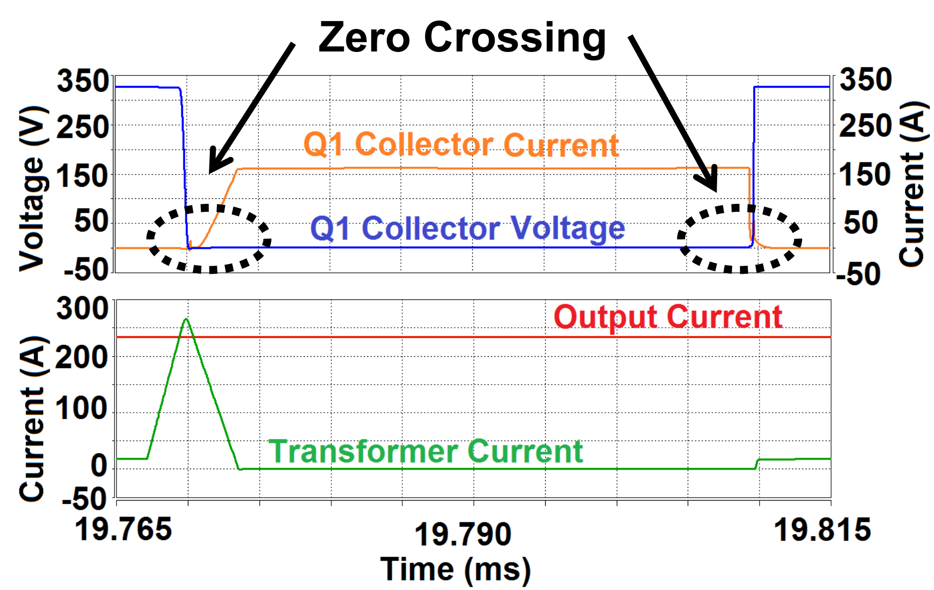
P_{out} : 20 kW
f_{out}: 60 Hz
f_{sw} : 20kHz
I_{out}: 160 A
V_{bus}: 114 V

Analysis: Inverter Electro-thermal Simulation - VTech Module Electrical Waveforms





A variable timing scheme that uses a voltage sensing circuit to detect the zero voltage crossing condition is used to determine the main switch turn-on time. The transformer current allows enough energy to discharge the main device (Q1) voltage to zero prior to main device conduction, enabling the zero-voltage switching condition.

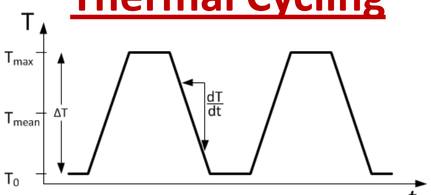


Application: Package Reliability Prediction

Physics-of-Failure Models

- Coffin-Manson
- Norris-Landzberg
- Energy Partitioning
- Strain-Range Partitioning

Variable Ramp-Rate Thermal Cycling

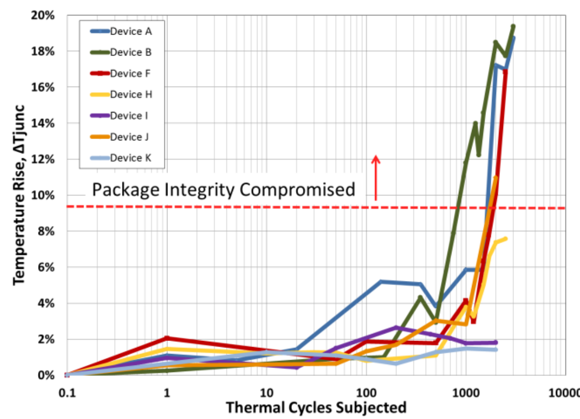


Mean Temp.	Temp. Swing	Dwell Time
$T_{av,1}$	ΔT_1	$t_{dw,1}$
$T_{av,2}$	ΔT_2	$t_{dw,2}$
…	…	…
$T_{av,i}$	ΔT_i	$t_{dw,i}$

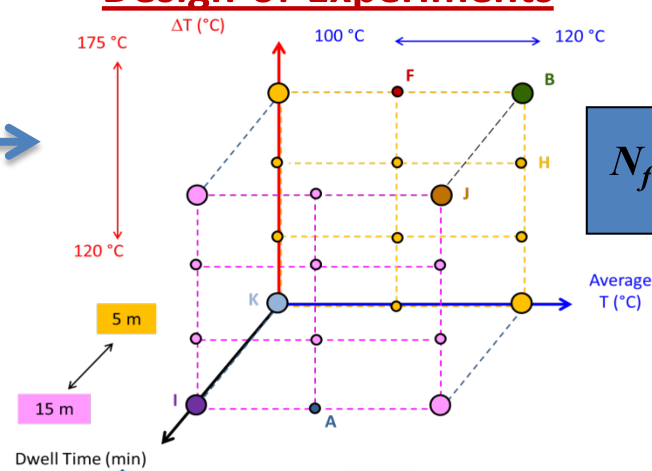
Multiple cycling parameters for each DBC stack construction.

High-speed Transient TSP

Used to detect changes in thermal resistance of buried-interfaces caused by thermal cycling damage.

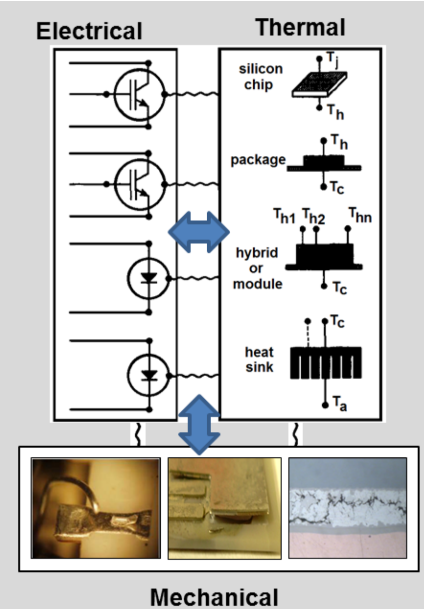


Degradation and Monitoring Design-of-Experiments



$$N_f(T_{av}, \Delta T, t_{dw})$$

Reliability Simulations



Technology Dependent Reliability Models

Summary

- Validated short circuit simulations form 1200V SiC MOSFET and Delphi Viper for full range of short circuit fault conditions: collector voltages, gate-drive parameters, and initial temperatures.
- Electro-thermal-mechanical simulations used to evaluate thermal stresses in Delphi Viper double-sided cooling power module for nominal and fault operating conditions.
- Performed a range of thermal cycling and thermal shock degradations to characterize mechanical reliability of two DBC stack types.
- Used new enhanced TSP measurement system to validate thermal cross-coupling between die within VA Tech soft switching modules.
- Performed full electro-thermal simulations and validations for VA Tech soft switching module in propulsion inverter operation at P_{out}= 50 kW @ 20 kHz.
- Will investigate using NREL bonded interface reliability characterization