

High-Dielectric-Constant Capacitors for Power Electronic Systems*

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Project ID# APE-008

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Overview

Timeline

- Project start date: FY05
- Project end date: FY13
- Project continuation & direction determined annually by DOE
- Percent complete: 85%

Budget

- Total project funding (FY10-FY13)
 - DOE: \$6260K (+ \$490K for equipment). Out of this total, \$520K was subcontracted to Penn State University
- Funding received in FY12: \$1950K
- Funding for FY13: \$800K (additional \$290K co-funded by Propulsion Materials Program)

Barriers addressed

- **A & C (Cost & Weight): Overall size and cost of inverters**
Capacitors are a significant fraction of the inverter volume ($\approx 35\%$), weight ($\approx 23\%$), and cost ($\approx 23\%$).
- **D (Performance & Lifetime): High-temperature operation**
The performance and lifetime of capacitors available today degrade rapidly with increasing temperature (ripple current capability decreases with temperature increase from 85°C to 105°C).

Partners

- Penn State University
- Delphi Electronics & Safety Systems
- Project Lead: Argonne National Laboratory

Relevance - Objectives

- **Overall objective:** Build and test ceramic capacitor prototype with high volumetric efficiency & high temperature capability. Pb-La-Zr-Ti-O (PLZT)-based ceramic capacitors are capable of operating at 140°C and 650 V (Advanced Power Electronics & Electric Motors – APEEM Goal).
- **Addresses targets:** This research directly addresses the size, cost & high-temperature requirements for DC bus capacitors in advanced power electronic modules in electric drive vehicles. Future availability of advanced high-temperature inverters will advance the application of highly fuel-efficient electric drive vehicles in the marketplace.
- **Specific objective for March '12 – March '13:** Fabricate & characterize a $\approx 10 \mu\text{F}$ multilayer capacitor. Identify & establish high-rate deposition process to reduce cost by making thicker high-voltage capable PLZT films.
- **Uniqueness/impact:** Our approach uses PLZT films that have high dielectric constant ($k \approx 100$), high breakdown field ($> 200 \text{ V}/\mu\text{m}$), & high insulation resistance ($> 10^{13} \Omega\text{-cm}$) and will meet APEEM requirements for capacitors operating at high temperature with high volumetric efficiency.

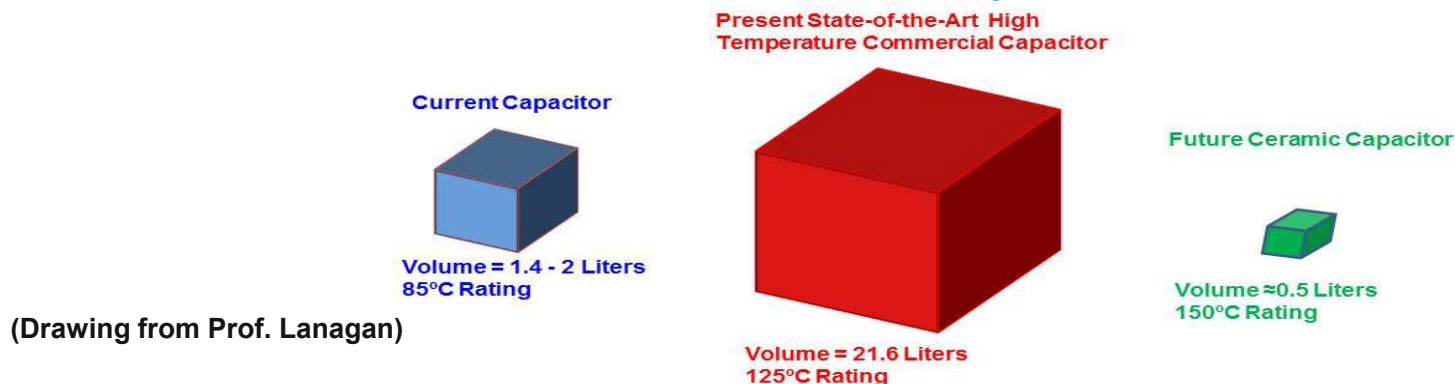
Milestones

Month/Year	Milestones or Go/No-Go Decision	Progress Notes
Oct. 2012	Fabricate a high-voltage-capable, prototype multilayer capacitor.	Fabricated multilayer capacitor with capacitance of 8.5 μF (unbiased) and 3.0 μF at 100 V (Slides 9 & 10).
Apr. 2013	Establish aerosol deposition (AD) system to fabricate PLZT films at high deposition rates at room temperature.	Installed AD system with X-Y-Z table, aerosol generator, particle size analyzer, & laser doppler velocimeter to measure particle speed during deposition (Slide 11).
July 2013	Synthesize sub-micron PLZT powder, and prepare inks for ink jet printing by Delphi.	Sub-micron powders have been synthesized and characterized, & inks have been made and delivered to Delphi for their evaluation.
Dec. 2013	Fabricate thicker films by AD process and make & test multilayer capacitor at operating voltages >450 V.	Deposited $\approx 3\text{-}\mu\text{m}$ -thick film in 20 min (vs. more than a day by spin coating process) and characterized its properties. Process needs to be optimized (Slide 12).

Technical Approach/Strategy

- Our approach is to develop high-dielectric-constant, high-temperature ceramic (Pb-La-Zr-Ti-O, PLZT) films on base-metal foils (“film-on-foil”) and establish high-rate deposition process to economically make these advanced capacitors.
 - PLZT’s ESR (related to dielectric loss) decreases with temperature.
 - Integration of base-metal (Al, Ni, Cu) electrodes provides significant cost & heat transfer advantages.
 - PLZT has a wide operating temperature range (suitable for SiC/GaN).
 - PLZT has low leakage currents due to material selection.

Volume of 1000 μF 600V capacitors in a Hybrid Electric Power Converter



Argonne's project addresses the technology gap in an innovative manner

Uniqueness of Project and Impact

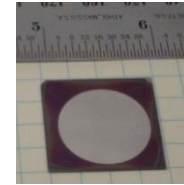
- **Specifications for “On-the-Road” technology capacitor (State-of-the-Art)**

- Volume of 2010 Prius cap. (888 μF) module, 85°C rating ≈ 1.5 L; 2011 Hyundai Sonata cap. (680 μF) module ≈ 1 L
- Limited to temperature of $\approx 85^\circ\text{C}$; ripple current capability degrades rapidly at temp. $>85^\circ\text{C}$

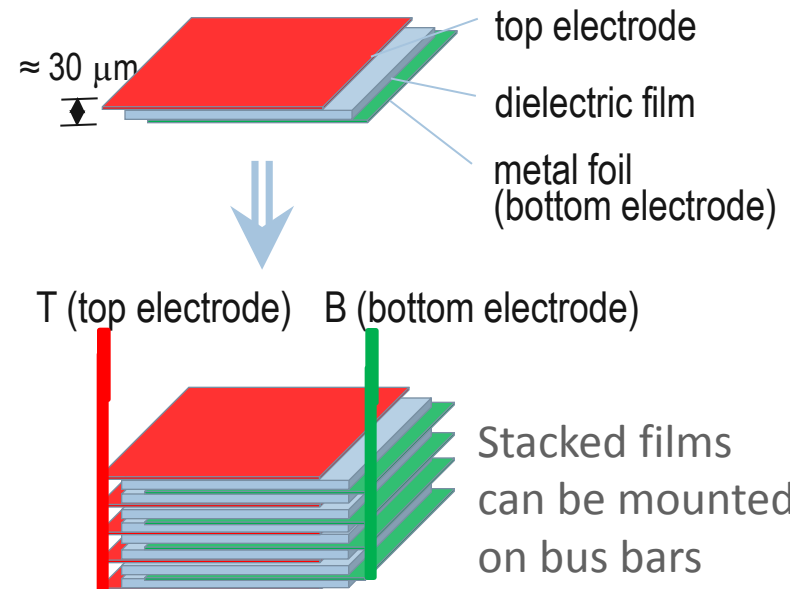
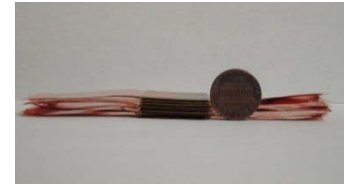
- **PLZT film-on-foil capacitor projected performance**

- Dielectric volume for a 1000 μF /450 V capacitor is ≈ 0.5 L (high degree of volumetric efficiency)
- No ripple current decrease between 85°C and 150°C. Projection is based on measured high temperature dielectric loss data
- Possible to make wound capacitors (Slide 19)
- Stacked and/or embedded capacitors significantly reduce component footprint, improve device performance, and provide greater design flexibility

Film-on-foil capacitor (FoF)

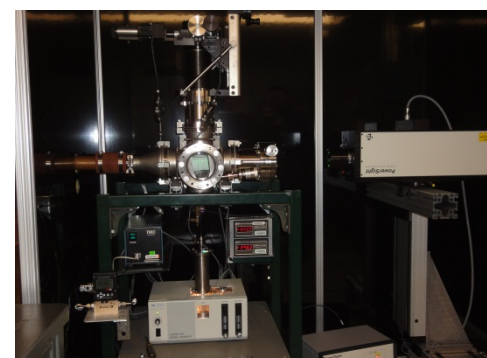
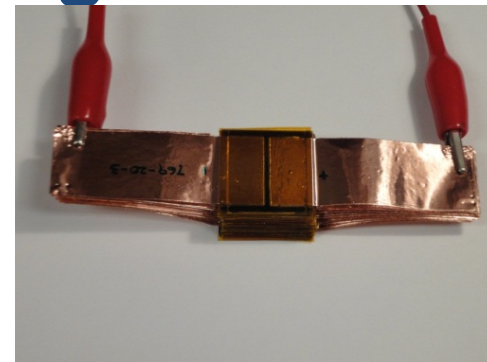


Stack of FoFs



Technical Accomplishments & Progress

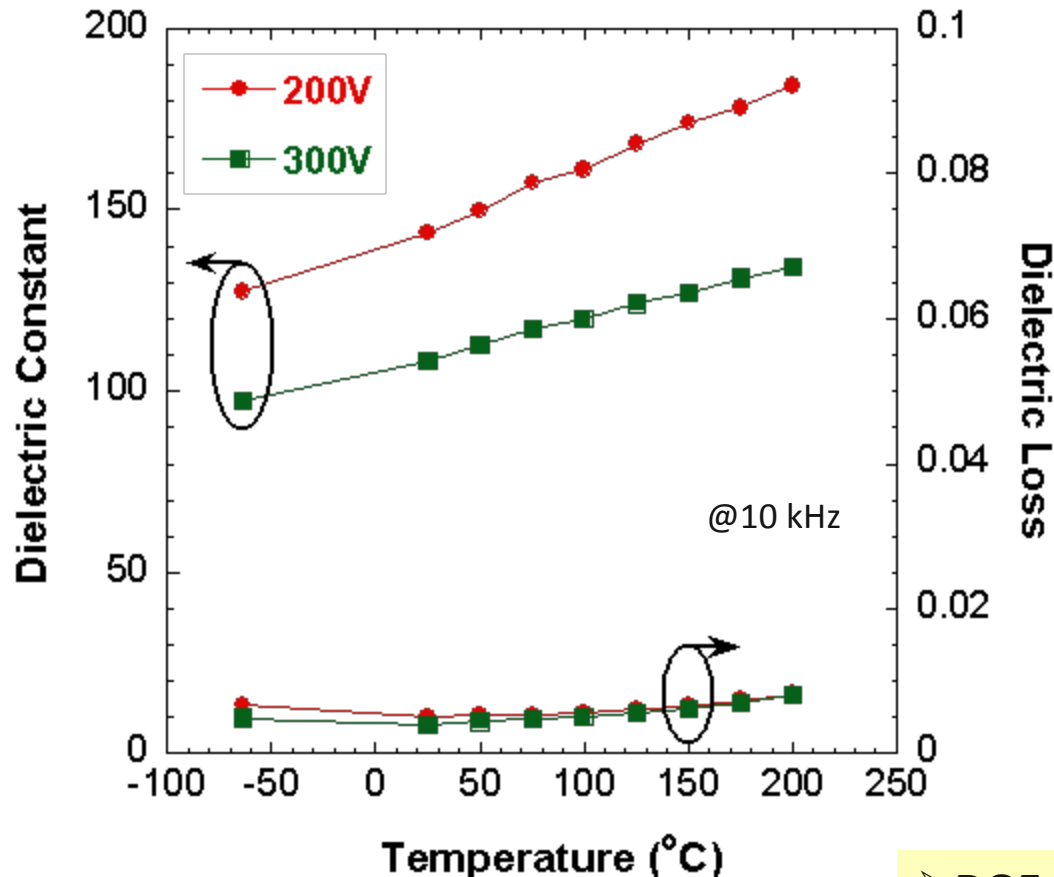
- Measured $k \approx 110$ & loss ≈ 0.004 (0.4%) at 300 V bias on a ≈ 3.0 μm -thick film (for comparison, $k \approx 3$ for polymer films). *Addresses the APEEM target for capacitor size.*
- Dielectric properties under bias (300 V) show an increase in k and decrease in loss with temperature increasing from -50°C to $+150^\circ\text{C}$. *Addresses APEEM temperature goal for capacitors (140°C).*
- Fabricated/characterized multilayer capacitor with capacitance of 8.5 μF (unbiased) and 3.0 μF at 100 V. *Addresses the APEEM goal for capacitor ESR.*
- Installed aerosol deposition system to fabricate PLZT films at high deposition rates. *Addresses APEEM requirements for low cost.*
- Developed solution chemistry and synthesized & characterized PLZT submicron powders for ink jet printing by Delphi. *Addresses APEEM requirements for low cost.*
- 55 publications and presentations have been made. One patent was issued & four patent applications were filed.



PLZT films have properties suitable for application in high-temperature inverters -- meeting the APEEM goals for temperature & high volumetric efficiency

Technical Accomplishments/Results (Cont.)

High temperature properties - PLZT/Ni



Measured $k \approx 110$ & loss ≈ 0.004 (i.e., 0.4%) @ 10 kHz & 300 V bias at room temperature on a 3 μm thick PLZT on Ni-foil

$\text{ESR} = \text{DF}/2\pi f c$ (DF = loss factor; f = frequency; c = capacitance).

Calculated ESR for 1000 μF cap. based on measured material properties

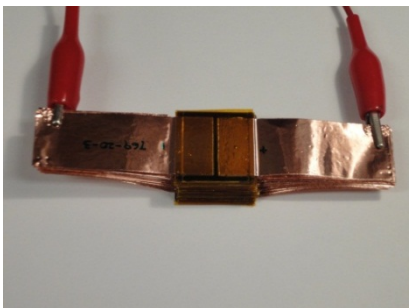
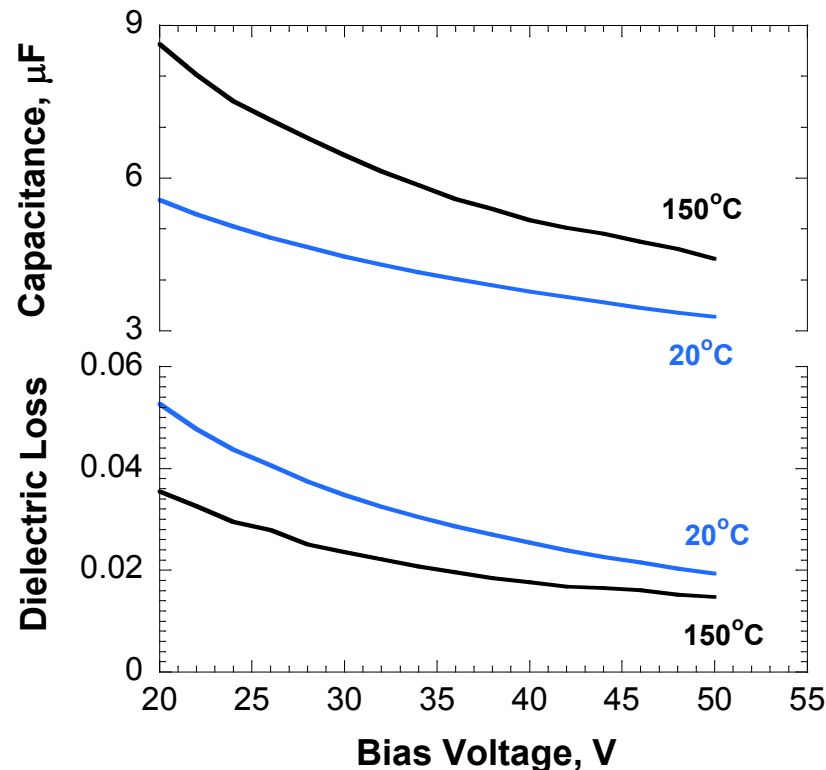
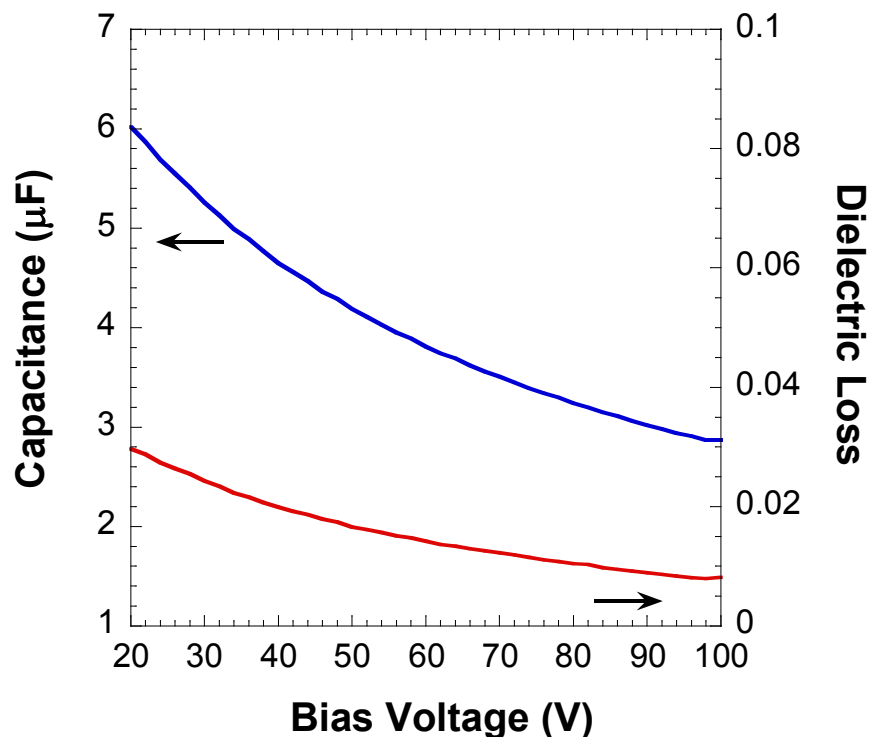
Bias Voltage (V)	ESR @ -64°C (m Ω)	ESR @ RT (m Ω)	ESR @ 150°C (m Ω)
200	0.11	0.08	0.10
300	0.08	0.06	0.10

➤ DOE-VT DC Bus Capacitor Goal ≤ 3 m Ω

ANL's film-on-foil has high dielectric constant at high voltages and high-temperature capability.

Technical Accomplishments/Results (Cont.)

Fabricated Multilayer Capacitors



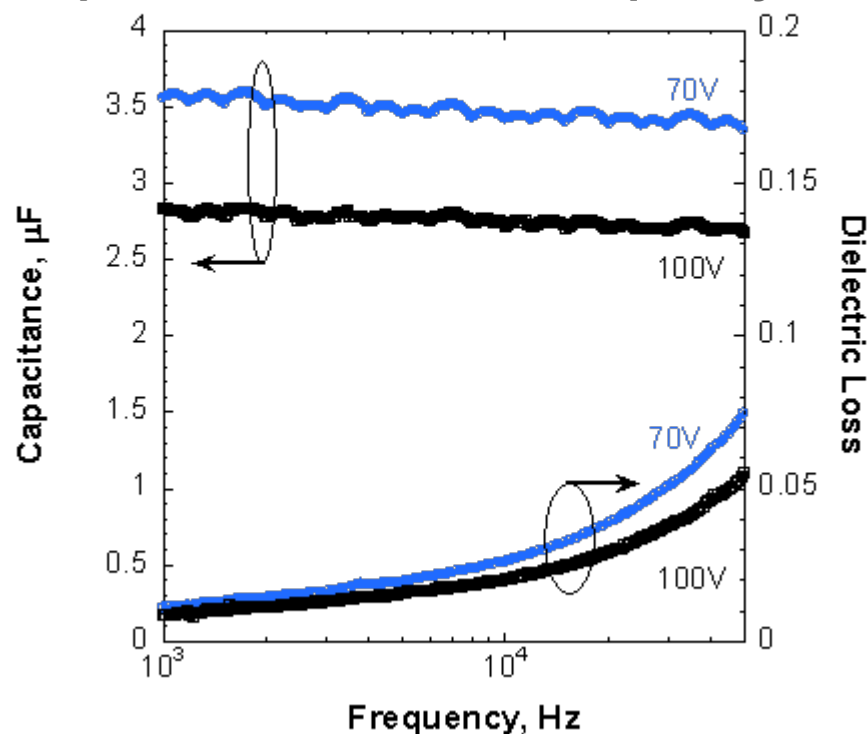
Extrapolated ESR of 1000 μF cap. based on properties measured on stack @ 50V: 0.3 m Ω @ 20°C & 0.23 m Ω @ 150°C

Film-on-foil multilayer capacitor has high-volumetric efficiency and low ESR in bias voltages.

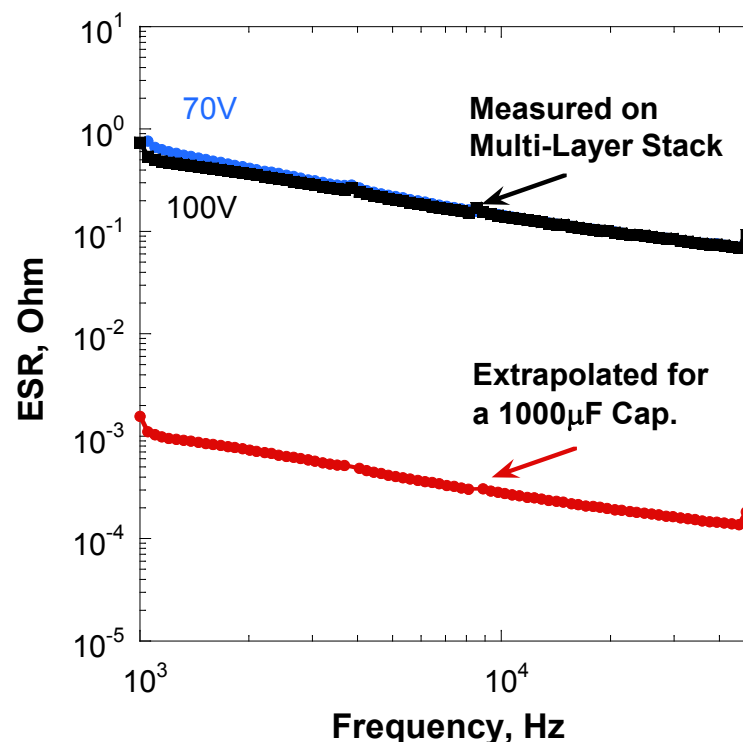
Technical Accomplishments/Results (Cont.)

Measured Capacitance & ESR of multilayer stacks

Capacitance & loss vs. frequency



ESR of Stack at 70 & 100 V



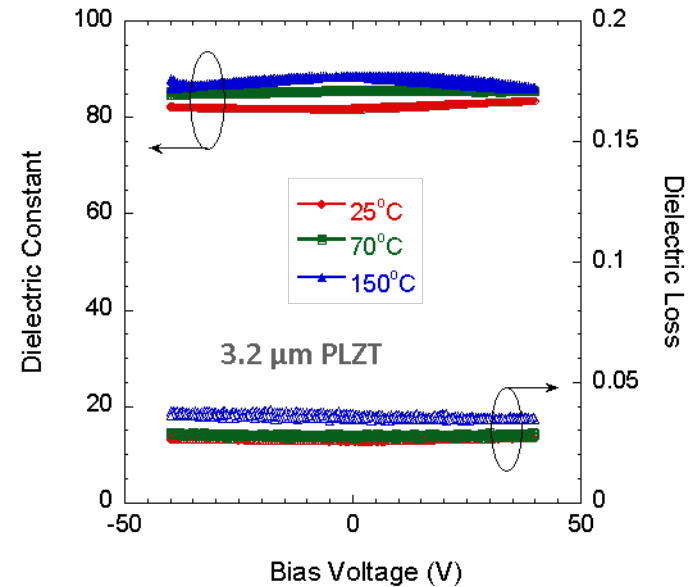
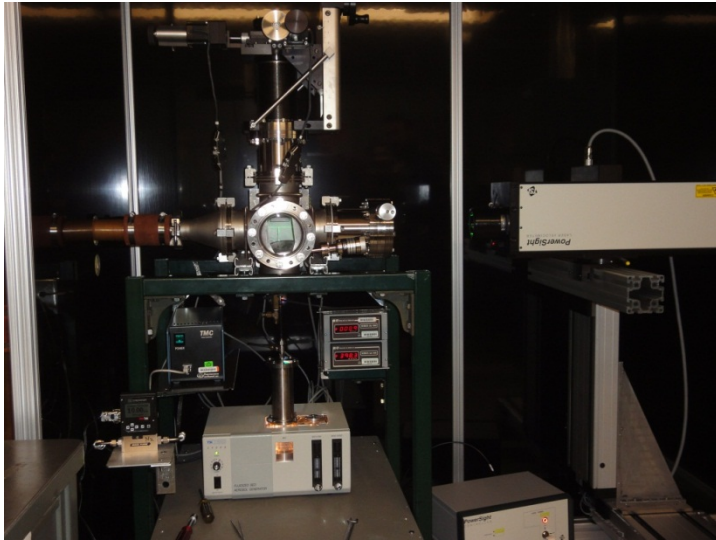
$$ESR = \frac{\tan\delta}{[2\pi f C]}$$

ESR for a 1000 μF cap. is ≤1 mΩ for >1kHz

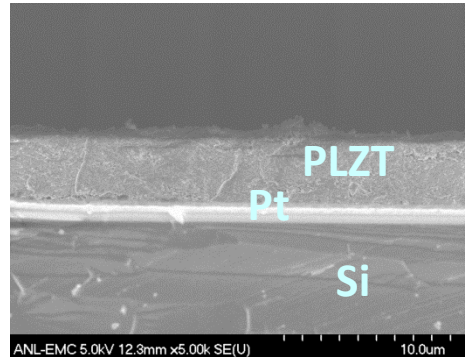
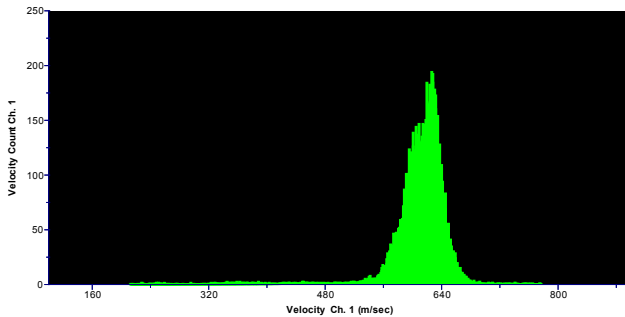
ESR of film-on-foil meets DOE-VT DC Link Capacitor Goal of ≤3 mΩ

Technical Accomplishments/Results (Cont.)

Aerosol (high-rate) Deposition of PLZT Films



Velocity 1 Histogram

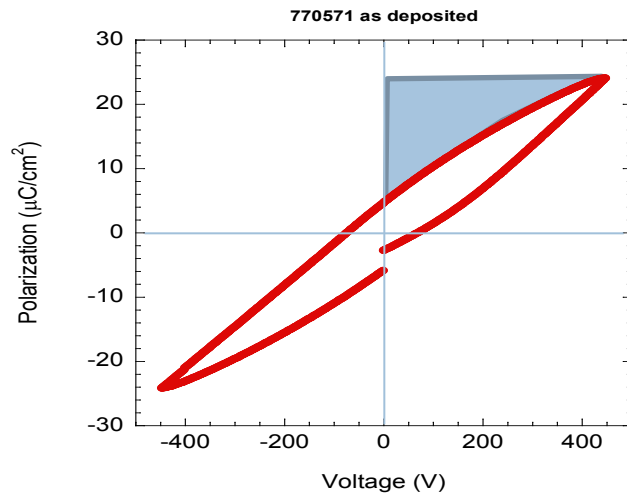
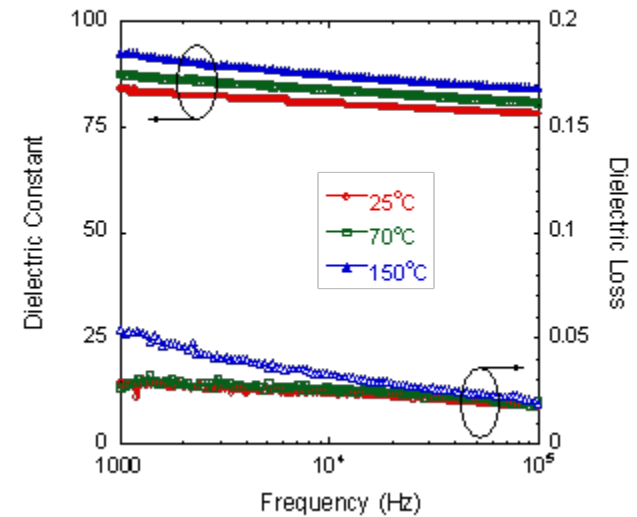
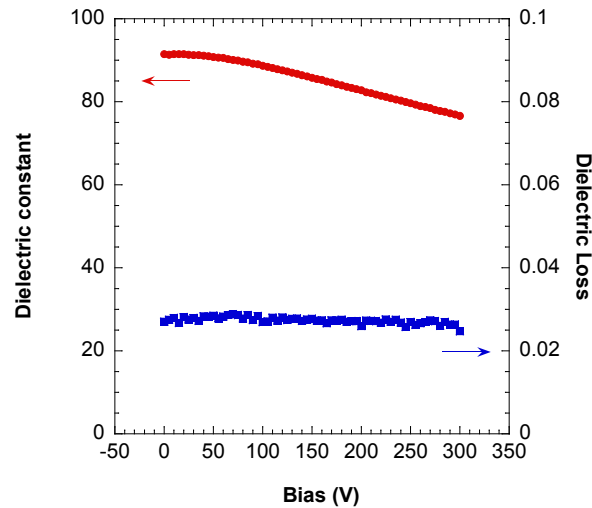
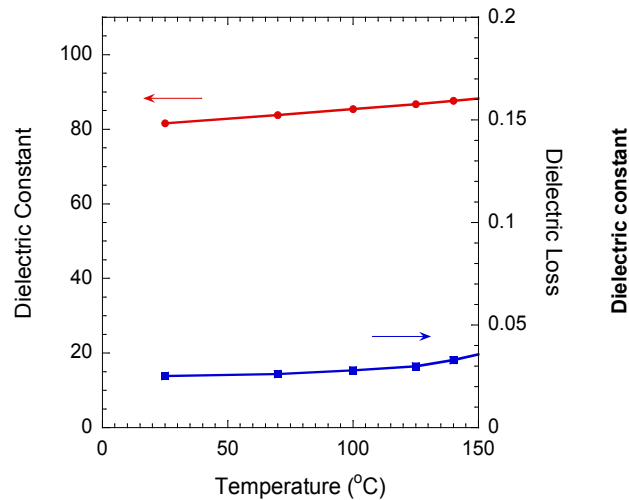


Deposited 3.2-μm-thick PLZT film in 20 min by AD (vs. more than a day by spin coating process)

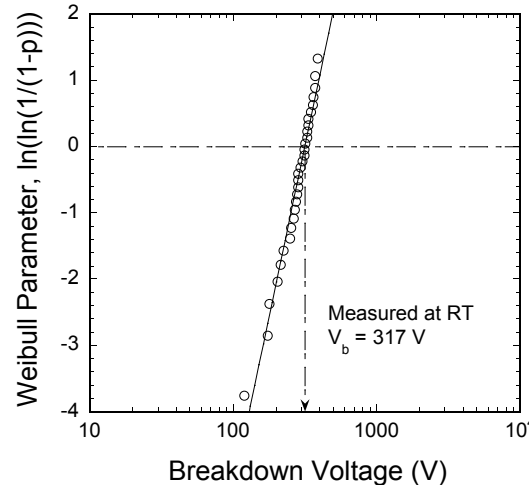
PLZT films with thickness >5 μm can be produced in few minutes on various substrates at room-temperature.

Technical Accomplishments/Results (Cont.)

Properties of 3.2- μm -thick PLZT deposited by AD Process



Recoverable energy density $\approx 11.7 \text{ J}/\text{cm}^3$



Preliminary results show that AD process has potential to significantly reduce the manufacturing cost.

Collaboration and coordination with other institutions



Dielectric characterization, reliability testing, electrode design & deposition, defining capacitor specifications & test protocol for APEEM



Industry partner/CRADA, inverter design engineering (direct customer for the technology), ink jet printing, stacking & connecting multilayer film-on-foils (Delphi works closely with a PWB manufacturer)



Electrode deposition, defining capacitor specifications & test protocol for APEEM



Strain tolerance of film-on-foils, independent validation of capacitor measurements

Proposed Future Work

The primary emphasis of our future work is on developing a process to: 1) make capacitors at faster rate to reduce manufacturing cost and 2) fabricate/characterize high voltage prototype capacitors (operating voltage of 450 V).

➤ **Optimize parameters of aerosol deposition process to fabricate thicker PLZT films capable of operating at 450 V (650 V transient).**

- Particle velocity, particle size distribution, deposition chamber pressure, carrier gas, nozzle design, and distance between nozzle & substrate

➤ **Develop process to produce sub-micron PLZT powders suitable for high-rate deposition processes.**

- Solution chemistry: Fuel/oxidant ratio, molar concentration of cations, type of fuel (citric acid, glycine, hydrazine)
- Post-synthesis processing of powders (calcining, ball milling) to produce particle size distribution appropriate for deposition

Proposed Future Work (Cont.)

- **Model heat generation/distribution issues (realistic thermal model to identify critical parameters required for long-term performance) in film-on-foils and multilayer PLZT capacitors.**
 - Finite difference 1-D modeling of capacitors using Matlab which incorporates conductive, convective, radiative thermal transport processes and dielectric loss generation
 - Higher dimensional finite element model (including field- & temperature-dependent properties) of PLZT film capacitors using Comsol to make model more accurate for high drive conditions

The primary emphasis of this work for the rest of this year and next year is on engineering and production scale-up.

Summary

We are developing dielectric films with increased capacitance density & capability for high temperature operation that have potential to reduce the size, weight, and cost of capacitors in inverters in electric drive vehicles – Addressing barriers A & C (cost & weight) and D (high-temperature operation)

- Demonstrated feasibility of material & approach to meet APEEM project objectives.
- Delphi feels that this material has strong potential for producing a very small, lower cost, very reliable and durable high-temperature bulk capacitor for automotive power electronics; however,
- The spin-coating process used to demonstrate material properties requires many processing steps and is slow.
- Aerosol deposition, a high-rate, room-temperature film deposition process, is being developed at Argonne to reduce capacitor cost.
- Processes to produce sub-micron PLZT powders suitable for high-rate deposition processes are being developed.

Technical Back-up Slides



DC Bus Capacitor Goals

For Electric Drive Power Inverters

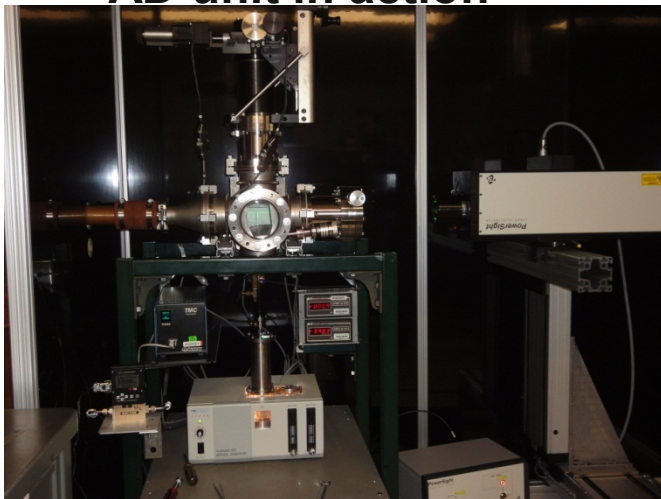
Typical Capacitor Bank Requirements

Capacitance, μF	1000 +10%; -0%
Operating voltage, VDC	450
Peak transient voltage, VDC for 50 ms	650
Leakage current at operating voltage, mA	≤ 1
Dissipation factor at 10 kHz ¹ , %	< 2
Equivalent series inductance (ESL), nH	≤ 5
Continuous ripple current, amp rms	90
Temperature range of ambient air, °C	-40 to +140
Volume requirement, l	≤ 0.6
Cost	$\leq \$30$
Failure mode	Benign
Life @ operating conditions, hr	$> 13,000$

¹ESR = $DF / 2 \pi f C$ where DF is dissipation factor and f is frequency

Aerosol Deposition (AD) of PLZT on Flexible Substrates

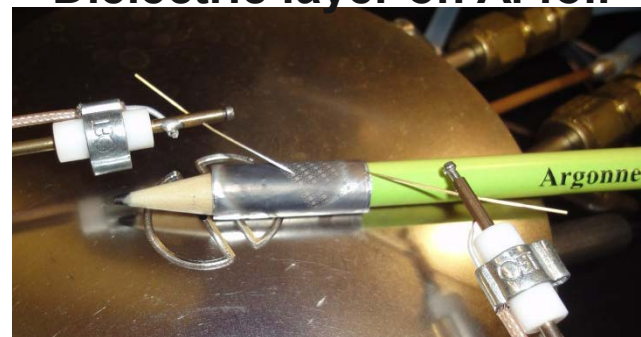
AD unit in action



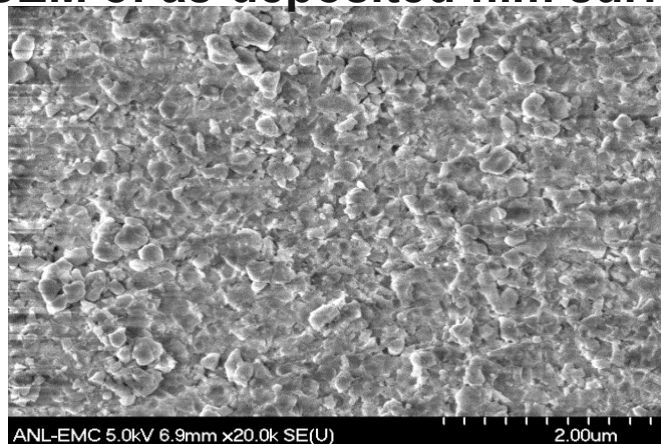
Al foil



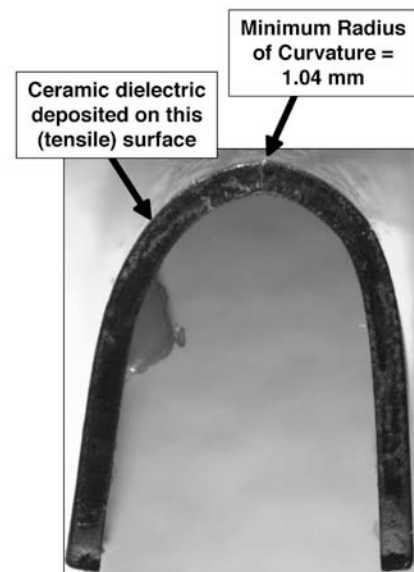
Dielectric layer on Al foil



SEM of as-deposited film surface



AD process has potential to produce wound ceramic film-on-foil capacitor



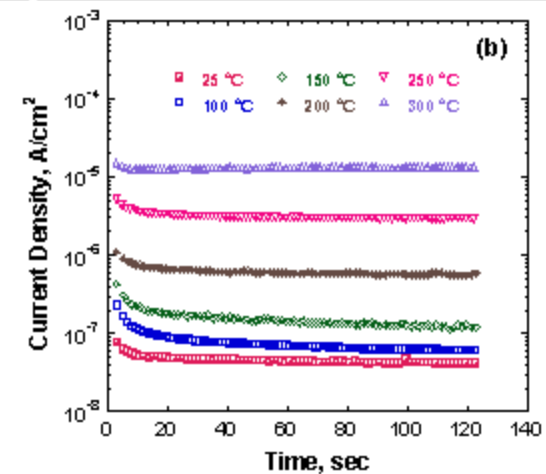
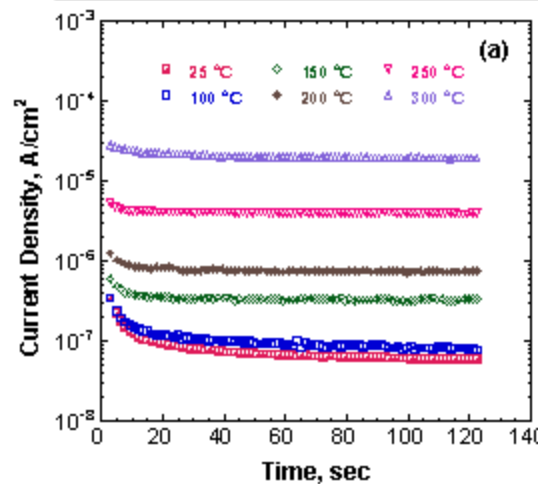
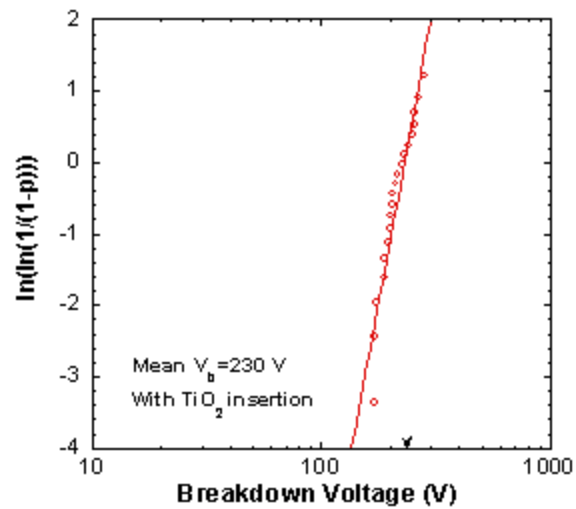
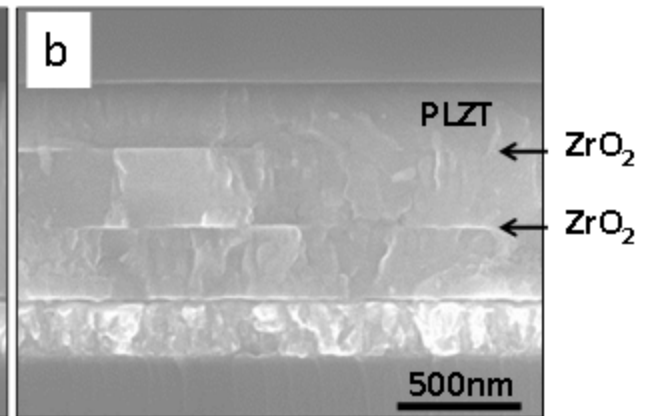
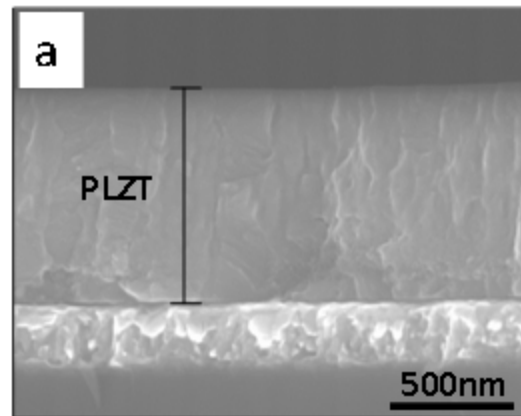
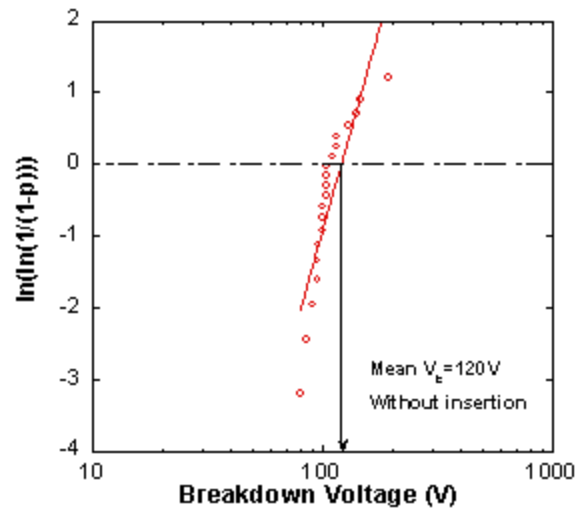
Strain-tolerance of film-on-foil
Measured by Andy Wereszczak (ORNL)

AD process will lower the capacitor manufacturing cost

Traditional Multilayer Ceramic Capacitors (MLCC) vs. Film-on-Foils

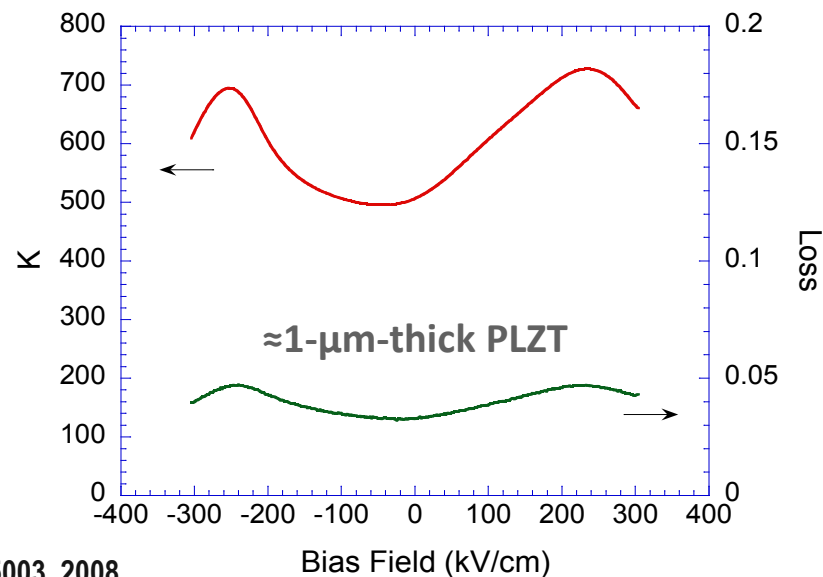
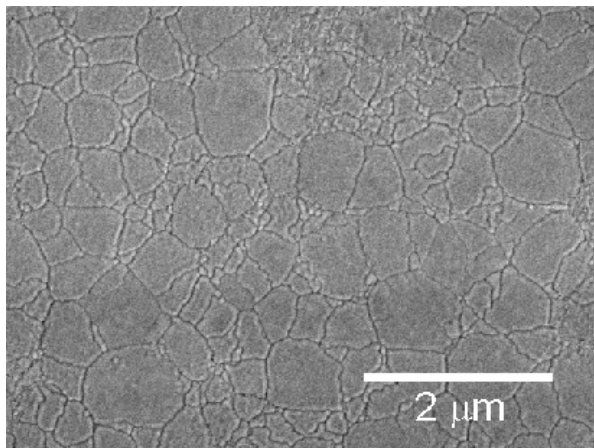
- In MLCCs, dielectric & electrode layers are co-fired at elevated temperatures; electrode layers are too-thick
- No benign failure mechanism in MLCCs (used in microelectronic applications)
- In film-on-foil approach, very thin electrodes are deposited at/near room temperature; possible to choose a wide range of electrode materials
- Benign failure mechanism is available with film-on-foils
- A variety of substrate materials (Al, Ni, Cu, Si) can be used in the film-on-foil approach
- Film-on-foils can tolerate certain bend radius
- Film-on-foil approach can produce wound ceramic capacitors

Enhancement of Dielectric Properties of PLZT via Superstructure Film Growth



- Improved dielectric properties with insertion of thin intermediate layers
- 2X improvement in breakdown strength
- ≈50% decrease in loss; decrease in leakage current

AFE $\text{Pb}_{0.92}\text{La}_{0.08}\text{Zr}_{0.95}\text{Ti}_{0.05}\text{O}_3$ Film Capacitors Grown on LNO Buffered Ni Substrates



Ref: Ma, Kwon, Narayanan, & Balachandran, J. Phys. D: Appl. Phys. 41, 205003, 2008.

