High-Dielectric-Constant Capacitors for Power Electronic Systems*

U. (Balu) Balachandran
Argonne National Laboratory

Team members at Argonne:
B. Ma, M. Narayanan, S. Liu,
S. Chao, S. Tong, S. E. Dorris

Project ID# APE008

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Overview

Timeline

- Project start date: FY05
- Project end date: FY13
- Project continuation & direction determined annually by DOE
- Percent complete: 70

Budget

- Total project funding
  - DOE share: 100%
- Funding received in FY10: $1800K
- Funding for FY11: $1750K

Barriers addressed

- **A & C (Cost & Weight): Overall size and cost of inverters**

  Capacitors are a significant fraction of the inverter volume (≈35%), weight (≈23%), and cost (≈23%).

- **D (Performance & Lifetime): High-temperature operation**

  The performance and lifetime of presently available capacitors degrade rapidly with increasing temperature (ripple current capability decreases with temperature increase from 85°C to 105°C).

Partners

- Penn State University
- Delphi Electronics
- Project Lead: Argonne National Laboratory

Relevance - Objectives

- Overall objective is to develop technology for fabricating high performance, economical, ceramic dielectric capacitors for power electronic systems in electric drive vehicles. The purpose is to build and test a capacitor prototype capable of operating at 140°C at 450 V.

  DC bus capacitors for inverters (DOE-APEEM Goals)

  – *(450 V, 1000 µF, <3 mΩ ESR, < 5 nH ESL, 100 A ripple current,140°C, benign failure)*

- Specific objective for May '10 – May '11 was to advance the proven laboratory scale technology to produce high-voltage (operating voltage 450 V) capable dielectric films on Ni foils ("film-on-foils") that will have the potential, upon scale-up, to meet DOE-APEEM goals.
- Dielectric films will have:
  – An operational temperature range of -50°C to +140°C
  – 450 V DC bus capability (peak transient 600 V)
  – High k (>100) under bias voltage of 450 V and breakdown strength (≈200 V/µm, i.e., ≈2 MV/cm) to meet weight & volume target

Relevance to Overall DOE Objectives of Petroleum Displacement

- Future availability of advanced high-temperature (together with lower cost, weight, & volume) inverters will advance the marketplace application of highly fuel-efficient & environmentally beneficial electric drive vehicles.
- Capacitors have direct impact on overall size, cost, & performance of inverters.
- Current polymer capacitors have temperature limitation.
- Capacitor development will reduce the size & increase the temperature of operation of one of the largest components in the inverter: the DC bus capacitor.

This project is developing dielectric films that, due to their increased capacitance density & better capability for high temperature operation, have potential to reduce the size, weight, and cost of capacitors in inverters (addressing barriers A, C, & D).

Milestones

Month/Year	Milestones or Go/No-Go Decision	Progress Notes
Oct. 2010	Go/No-Go Decision: Fabricate 1" x 1" film-on-foil dielectrics with uniform properties.	Fabricated larger area (20-mm dia.) dielectric film with capacitance of ≈3 μF @ 15 V/μm bias (Slide 9). Fabricated 1" x 1" film, deposited 5 mm dia. electrodes at different locations and measured uniform properties (Slide 21).
May 2011	Fabricate high-voltage-capable film-on-foils with high breakdown strength.	Fabricated ≈3-μm-thick dielectric film with breakdown strength of ≈270 V/μm, i.e., 2.7 MV/cm (average breakdown voltage of the sample ≈840 V) (Slide 11).
Sept. 2011	Fabricate a high-voltage-capable, ≈10 μF multilayer capacitor with end-termination.	Fabricated a 5 μF (unbiased) capacitor by stacking three film-on-foils (Slide 12). Because of the close proximity of the Cu ribbon terminals, we were not able to apply bias voltages. Lessons learned will help us to make the ≈10 μF device.
Dec. 2011	Identify fabrication methodology to reduce capacitor cost.	Produced films with factor of 5X increased rate. Properties need to be optimized (Slide 13).

Technical Approach/Strategy

- Develop ferroelectric (PLZT) dielectric film-on-foils that are either stacked on or embedded directly into the printed wire board.
- Integration of base-metal electrodes provides a cost advantage over noble metals used in conventional multilayer capacitors.
- Ferroelectrics possess high dielectric constants, breakdown fields, and insulation resistance. With their ability to withstand high temperatures, they can tolerate high ripple currents at under-the-hood conditions (slides 9-11).
- Stacked and/or embedded capacitors significantly reduce component footprint, improve device performance, achieve high volumetric and gravimetric efficiency, and offer an economic advantage (slide 7).
- Our approach focuses on fabricating films by chemical solution deposition, developing a fundamental understanding of processing effects on properties, and arriving at robust processing strategies to make prototype high-voltage capable multilayer devices.

Argonne's project addresses the technology gap in an innovative manner.

Uniqueness of Project and Impact
(caps embedded directly into PWB – caps are "invisible")

Basic Element

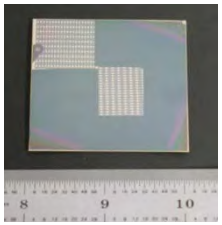
Metal foil coated with thin film Pb-La-Zr-Ti-Oxide (PLZT) dielectric

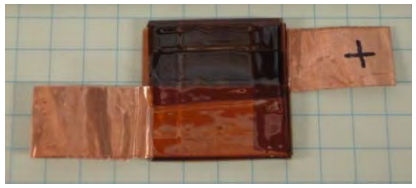
- **PLZT/Ni Film-on-Foil**
- **PLZT/Cu Film-on-Foil**

Component

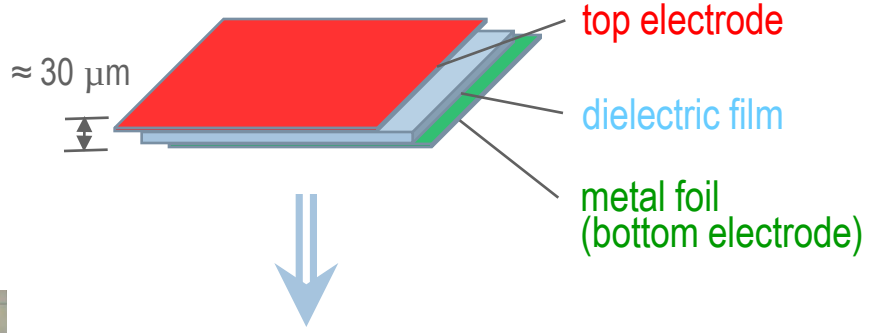
Stack on or embed coated foils directly into printed wire board (PWB) for power electronics in EDVs.

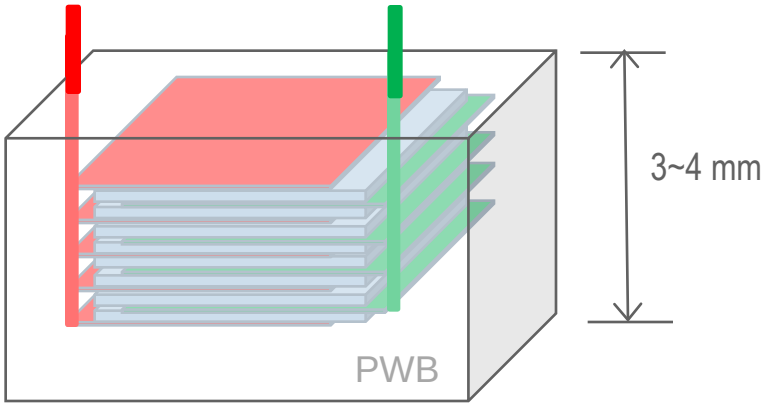
Film-on-foil capacitor (FoF)





Stack of three FoFs





Advantages

Reduces component footprint

Shortens interconnect lengths

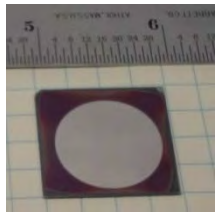
Reduces parasitic inductive losses & electromagnetic interference

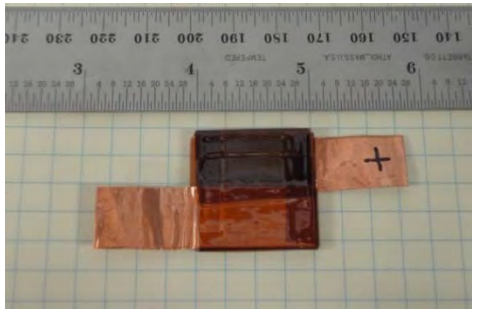
Embedded capacitor with interconnections

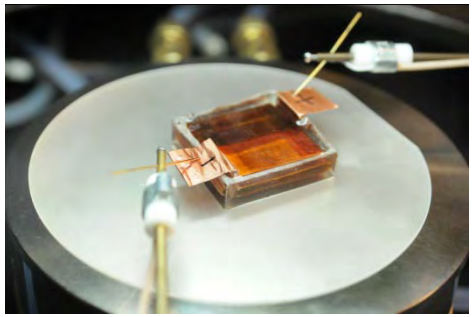
Reliability is improved because the number & size of interconnections are reduced. Solder joints that are most susceptible to failure are no longer needed.

Technical Accomplishments & Progress

- Fabricated a 20-mm diameter film-on-foil with capacitance of ≈3 μF under 15 V/μm bias (at the 2010 AMR meeting we reported capacitance of ≈0.5 μF under 15 V/μm bias).
- Fabricated ≈5 μF capacitor (unbiased) by stacking three 1” x 1” film-on-foils (capacitance density ≈4 μF/cm^3). We were unable to measure its capacitance under bias field using the LCR meter due to the close proximity of the Cu ribbon terminals. Lessons learned from this experiment will help us to make high-voltage capacitors.
- Measured dielectric constant k ≈120 & tan δ (dissipation factor) ≈0.008 under 300 V bias on a ≈3.0-μm-thick PLZT film (calculated k ≈90 under 600 V bias from the P-E loop measurement).
- Made film-on-foil with breakdown field ≈270 V/μm (≈2.7 MV/cm); average breakdown voltage ≈840 V on a ≈3.0-μm-thick film.
- Dielectric properties under bias field show an increase in k and decrease in loss with temperature increasing from -50°C to +200°C.
- Modified solution deposition process to produce PLZT films at ≈5 times faster compared to present rate; process needs optimization.
- Dielectric films are thermally cycled (about 1000 cycles) between -50°C and +150°C with no measurable degradation in k.
- Over 45 publications and presentations have been made. One patent was issued & two patent applications were filed.



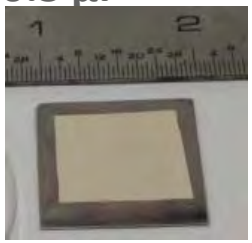




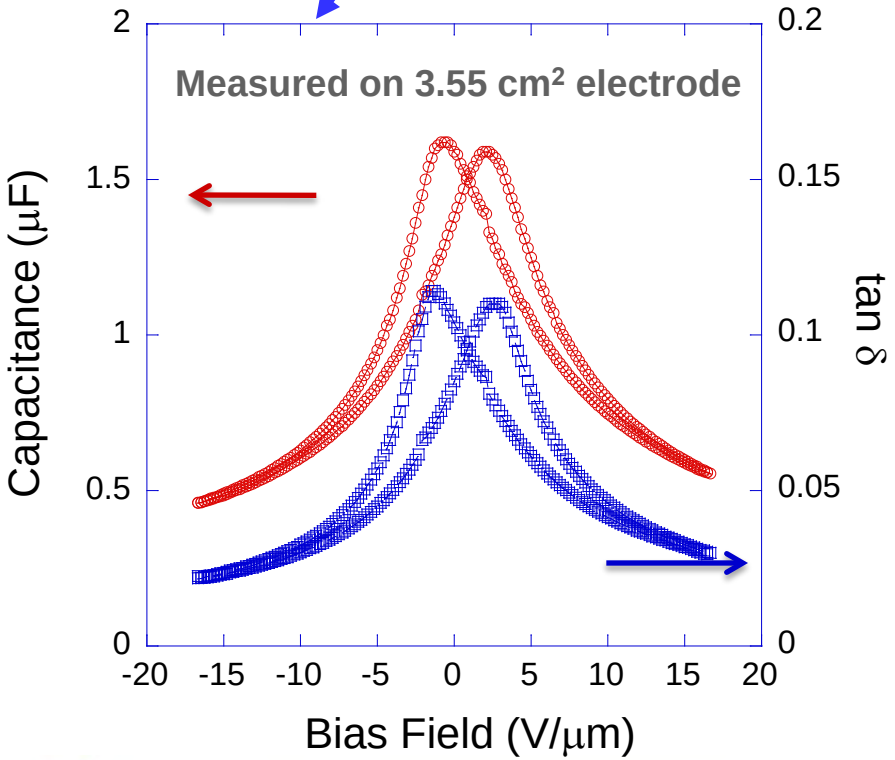
Technical Accomplishments/Results (Contd.)

Results @ '10 AMR Meeting (6/10/10)

- Results on larger area of dielectric films with capacitance of ≈0.5 µF @ 15 V/µm bias (unbiased capacitance ≈1.6 µF)

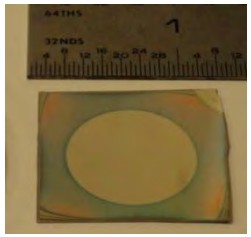


2010 AMR

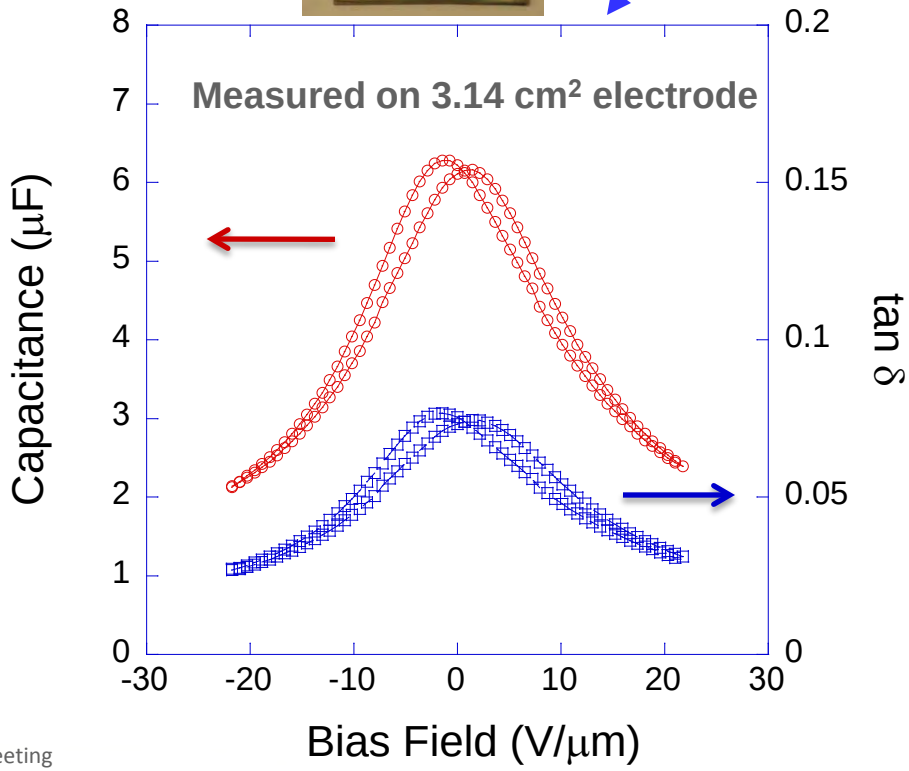


Results @'11 AMR Meeting (5/10/11)

- Results on larger area of dielectric films with capacitance of ≈3 µF @ 15 V/µm bias (unbiased capacitance ≈6 µF)

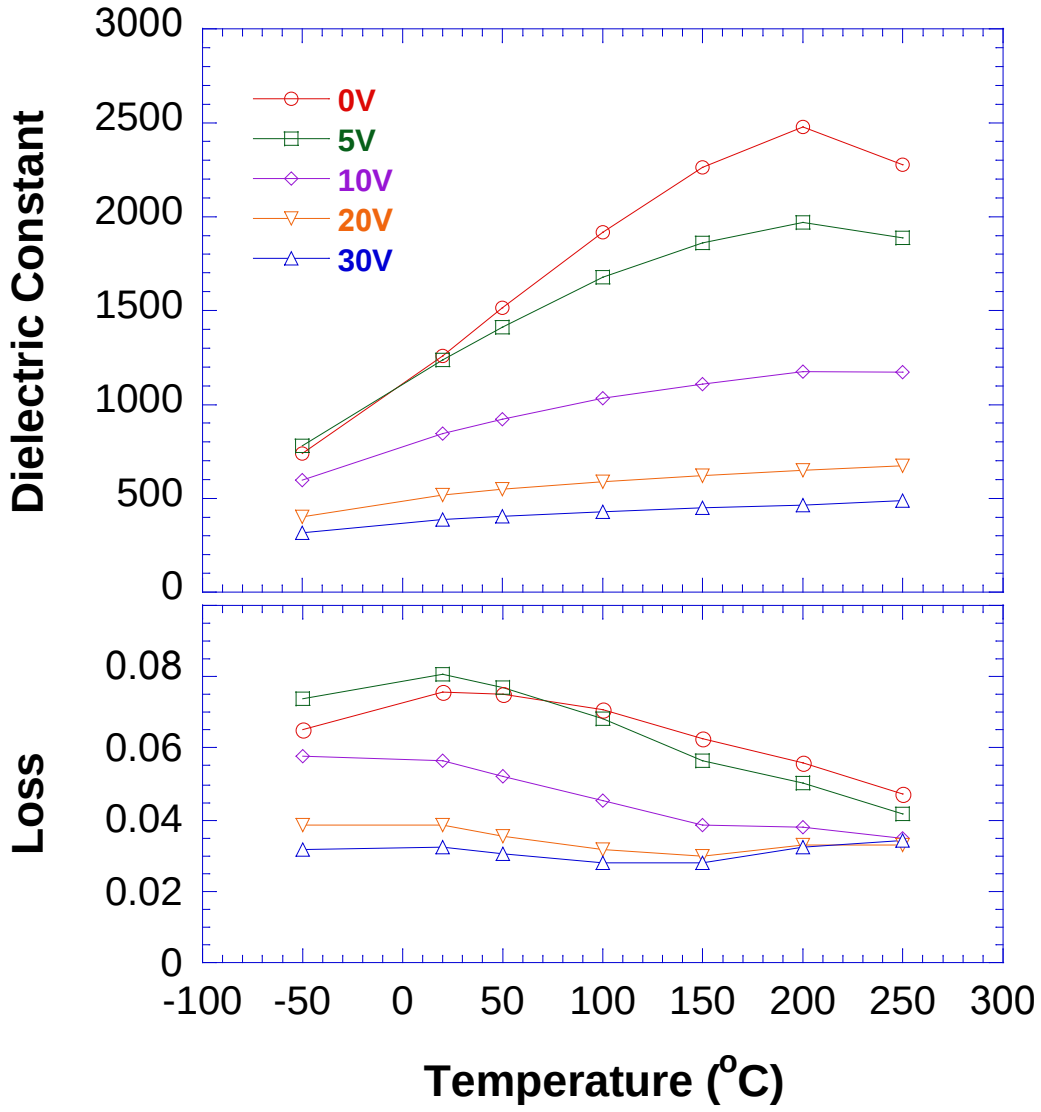


2011 AMR



Technical Accomplishments/Results (Contd.)

Temperature dependent properties - PLZT/Ni

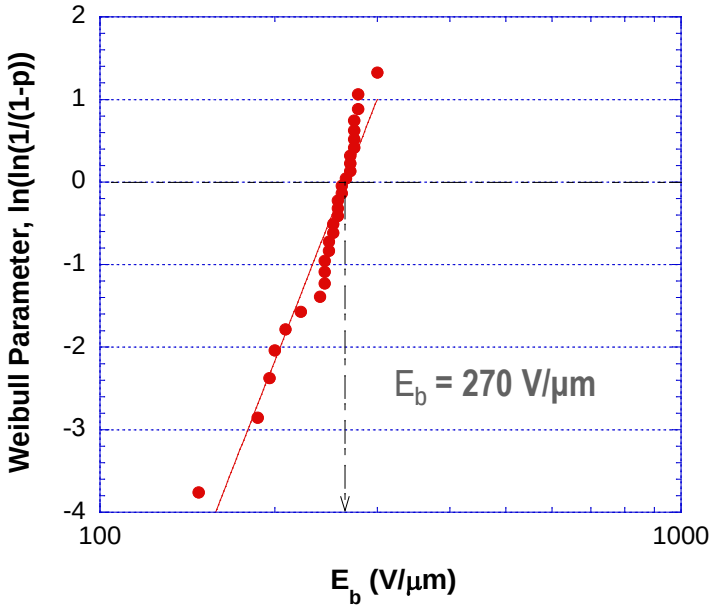


Measured k ≈120 & loss ≈ 0.008 (0.8%) @ 300 V bias at room temperature on a ≈3 μm thick PLZT on Ni-foil

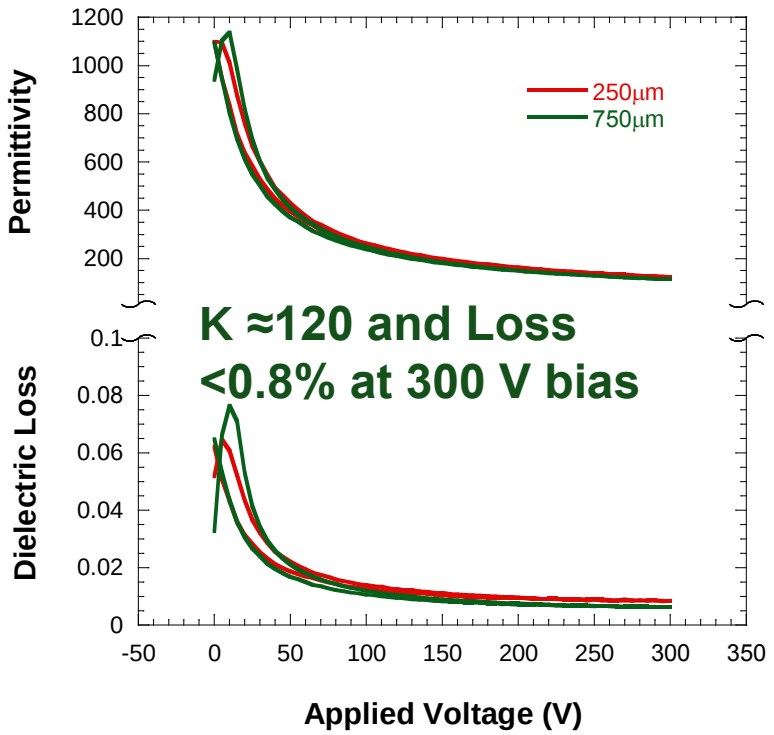
- Dielectric constant (capacitance) increases and loss decreases with temperature (-50 to +200°C).
- ESR = DF/2πfc (DF = loss factor; f = frequency; c = capacitance); ESR decreases.
- No decrease in ripple current capability up to 200°C; Projection based on measured capacitance and loss & preliminary HALT data at high temperatures.

Technical Accomplishments/Results (Contd.)

Breakdown strength & Dielectric properties as a function of bias voltage



(3-μm-thick PLZT on Ni Foil)

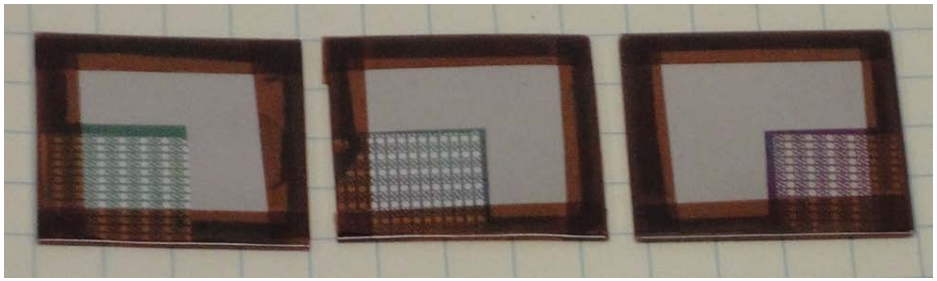


Average breakdown voltage of a ≈3.0 μm-thick PLZT film-on-foil is ≈840 V

- Higher E_b increases capacitance density, which reduces dielectric layer thickness & cost of the capacitors for inverter applications.
- Higher dielectric constant under bias field (k ≈120 at 300 V) provides greater volumetric efficiency compared to current polymeric films (k ≈6 at 300 V).

Technical Accomplishments/Results (Contd.)

Prototype Multilayer Capacitor with Leads



Measured capacitance (unbiased) ≈5 µF (cap. density ≈4 µF/cm^3)

For the fabrication we used:

- Three foils that were tested ≈1/4th area using small-size electrodes
- Ni foil thickness ≈400 µm
- Cap. of individual foils ≈1.7 µF (0 V)
- Four Cu shims (thickness ≈120 µm)
- Two Cu ribbons (thickness ≈80 µm)

(Due to the close proximity of the Cu foils, we were not able to apply bias voltages)

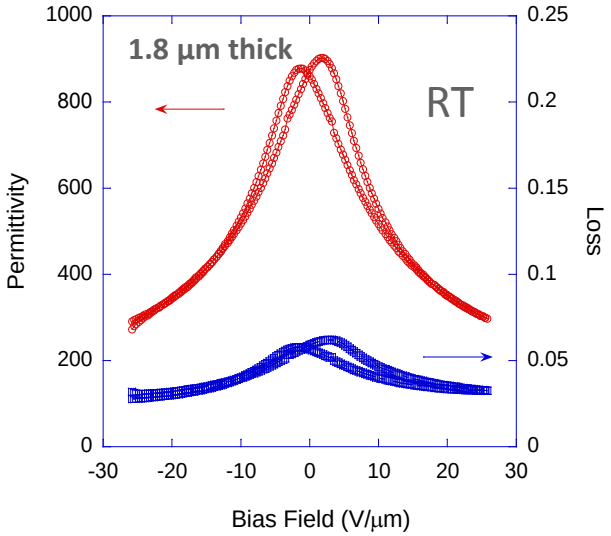
Calculation of the volume of 1000 µF/450 V Cap based on measured values at 300 V bias (slide 11) & k @ 600 V extracted from P-E loop measurement:

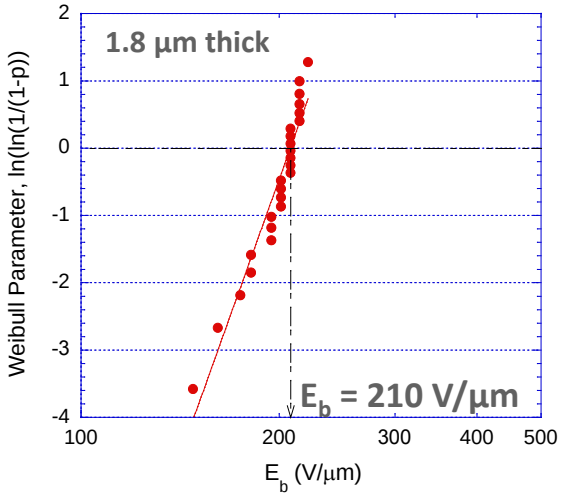
- Volume will be 0.55 L if ≈80 µm thick Ni foil & ½ oz. Cu ribbon (≈20 µm) is used.
- Volume can be reduced to <0.2 L if new, improved films (slide 9) are used.

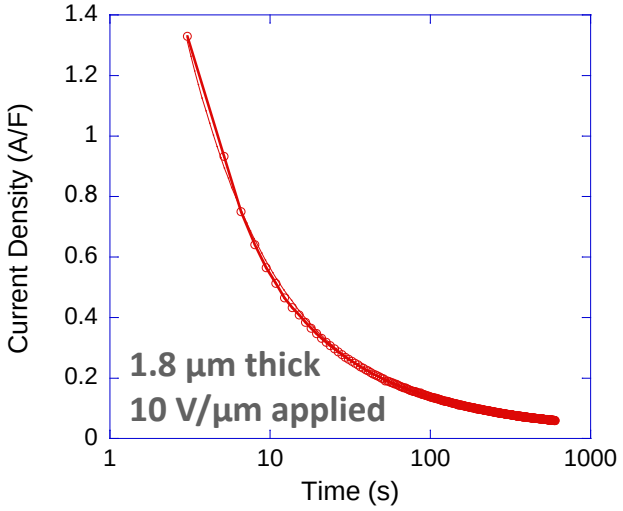
- DOE-OVT DC Bus Capacitor Goal ≤0.6 L
- Volume and capacitance of current polymer film capacitor module in Camry ≈2.6 L (2,098 µF) & Lexus LS 600h ≈4.0 L (2,629 µF). Ref: ORNL/TM-2007/190 & ORNL/TM-2008/185 reports.

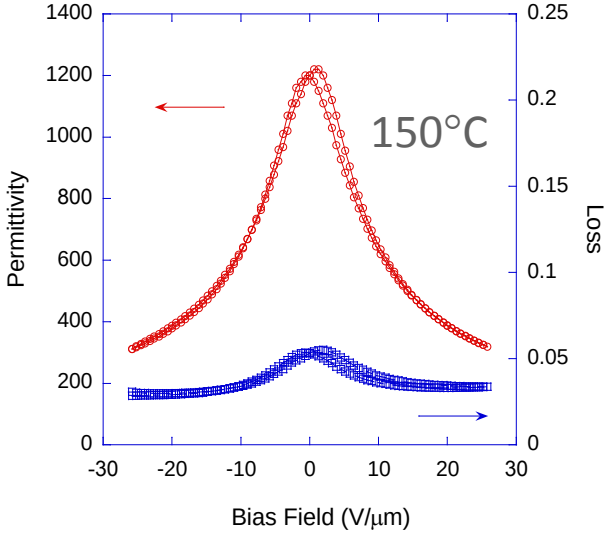
Technical Accomplishments/Results (Contd.)

Modified solution deposition process – ≈5x faster rate









- Film thickness per coating is ≈5 times that of conventional 2MOE processed films (decreases cost to make thicker films).
- Leakage ≈0.04 A/F (4 x 10^{-8} A/µF).
- Mean breakdown voltage E_b ≈210 V/µm.
- Process needs optimization.

Collaboration and coordination with other institutions

Dielectric characterization, reliability testing, electrode design & deposition, defining capacitor specifications & test protocol for APEEM

Industry partner/CRADA, inverter design engineering (direct customer for the technology), stacking & connecting multilayer film-on-foils (Delphi works closely with a PWB manufacturer)

Birck nano-tech center (BNC) to fabricate films, film process technology transfer to Delphi at BNC

Electrode deposition, defining capacitor specifications & test protocol for APEEM

Strain tolerance of film-on-foils

Started interacting with a manufacturer of multilayer ceramic capacitor but no formal agreement as of this date.

Future Work

The primary emphasis of our future work is on advancing the proven laboratory scale film-on-foil technology and fabricating ≈10 µF, high-voltage-capable (operating voltage of 450 V) capacitors.

- Optimize processing conditions to produce high-voltage-capable films.
- Investigate effects of electrode thickness & surface resistivity (Ω/☐), and optimize electrode design to share large ripple currents in a multilayer architecture.
- Stack pre-cleared (by applying voltages >600 V) film-on-foils, and produce ≈10 µF, 450 V capacitor.
- Characterize the dielectric properties & high temperature reliability.
- Using newly acquired sputter deposition system, investigate metal/metal oxide electrodes to obtain benign failure via solid-state control of conductor-insulator transition. This approach provides one avenue to obtain graceful failure mode in multilayer device.
- Optimize the new solution methodology (slide 13) to produce thicker films at faster rate to reduce capacitor cost.
- Collaborate with industrial partner to manufacture multilayer capacitors.

Summary

We are developing dielectric films with increased capacitance density & capability for high temperature operation that have potential to reduce the size, weight, and cost of capacitors in inverters in electric drive vehicles.

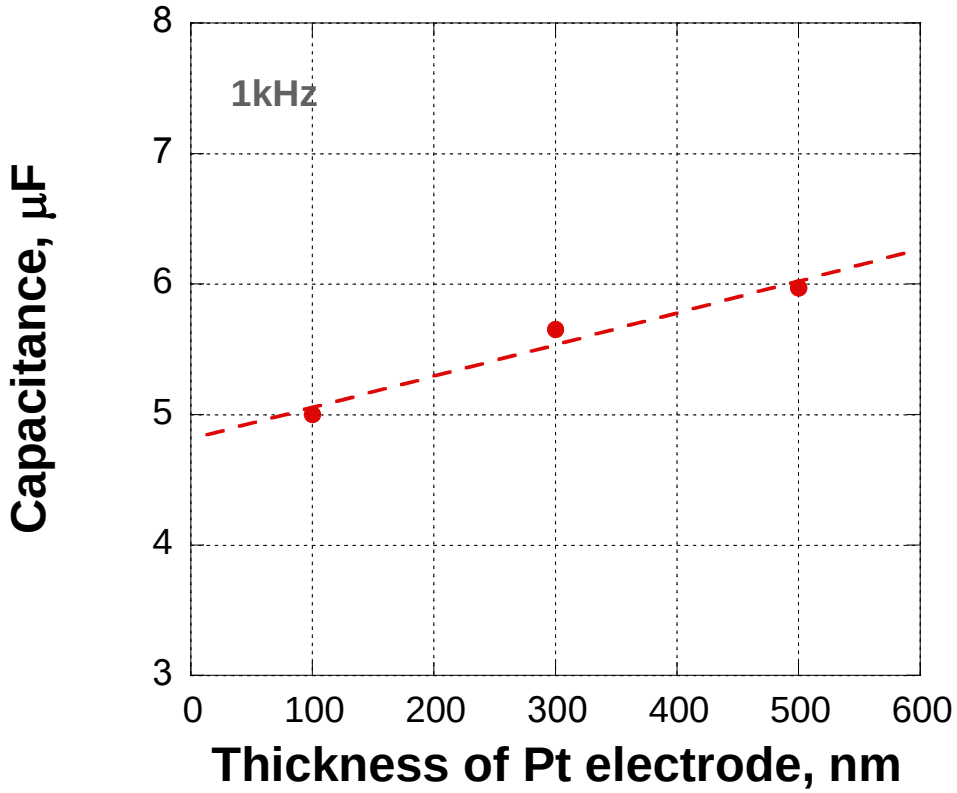
- We have made PLZT films with k ≈ 120 & loss ≈0.008 under 300 V bias; breakdown field ≈ 270 V/μm.
- We have fabricated a PLZT film (≈3.1 cm^2 area) with capacitance of ≈3 μF @ 15 V/μm.
- We fabricated ≈5 μF capacitor (unbiased) with end-termination.
- Based on measured capacitance & dielectric loss and preliminary HALT data at high temperatures, there is no decrease in ripple current capability up to 200°C.
- Based on measured values at 300 V, the volume of a 1000 μF/450 V capacitor will be 0.55 L (DOE-OVT goal ≤0.6 L).
- We are collaborating with partners to overcome the barriers of this technology for inverter application and to commercialize the technology.

At the end of FY11, we will have produced a high-voltage-capable ≈10 μF multilayer capacitor with end-termination.

Technical Back-up Slides

Electrode Thickness Effect

(Pt electrode diameter: 20 mm)



Electrode	Thickness (nm)	Ω/□
Pt	50	2.0
Pt	100	1.0
Pt	500	0.2
Al	50	0.5
Al	100	0.25
Al	500	0.05

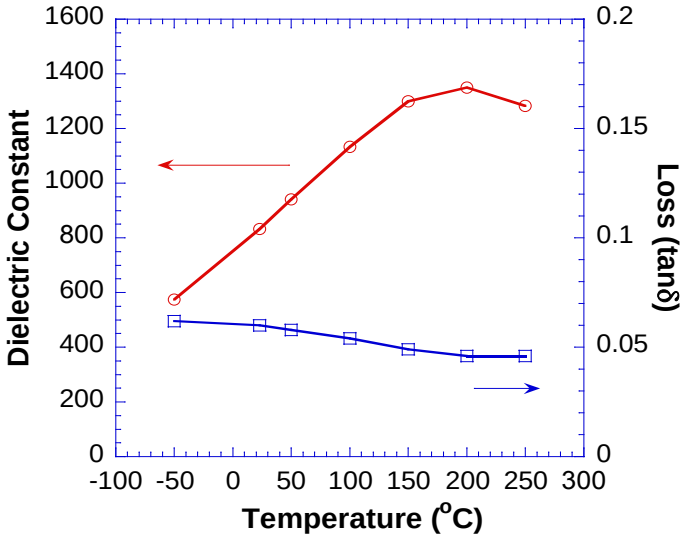
ρ of Pt = 1.05×10^{-7} Ω-m

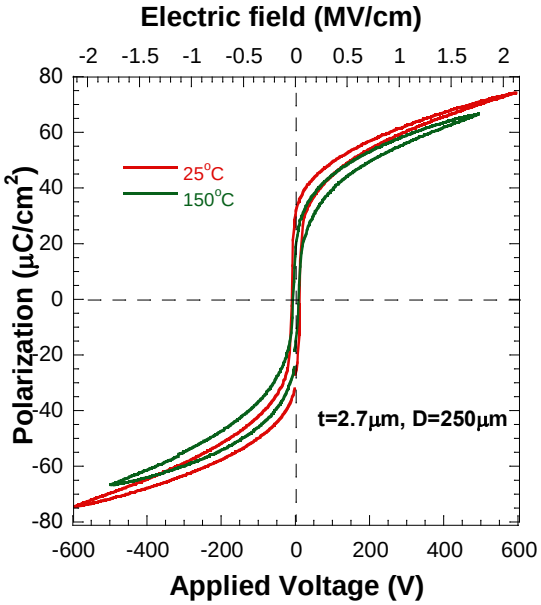
ρ of Al = 2.82×10^{-8} Ω-m

- **Electrodes should carry large currents and, at the same time, provide benign failure mode in multilayer architecture.**
- **Electrode surface resistivity is consistent with commercial polymer film capacitors carrying large ripple currents.**

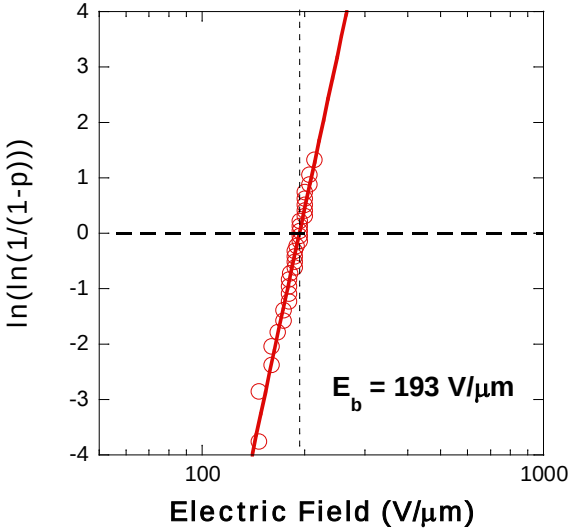
Technical Accomplishments/Results (Contd.)

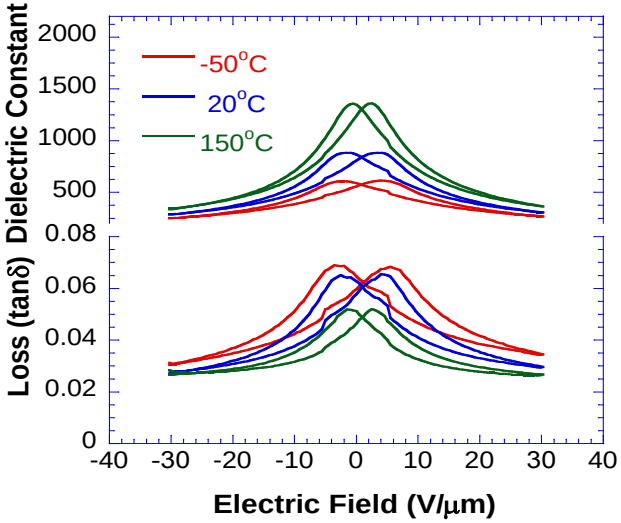
New solution chemistry for adaption by industry - 2MOE free





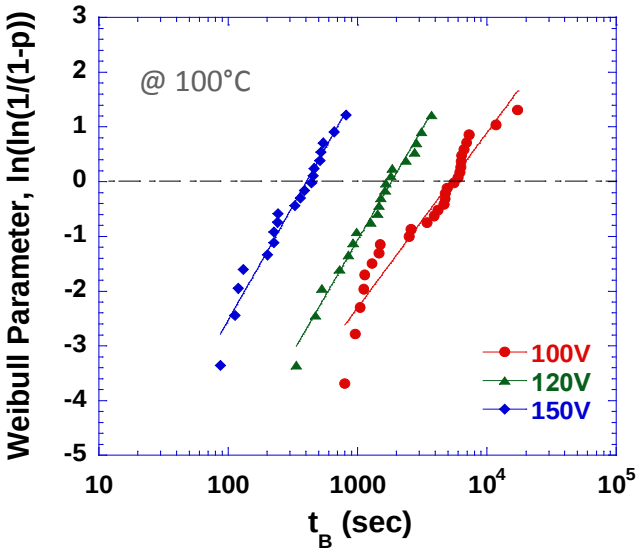
≈2.7-μm-thick film

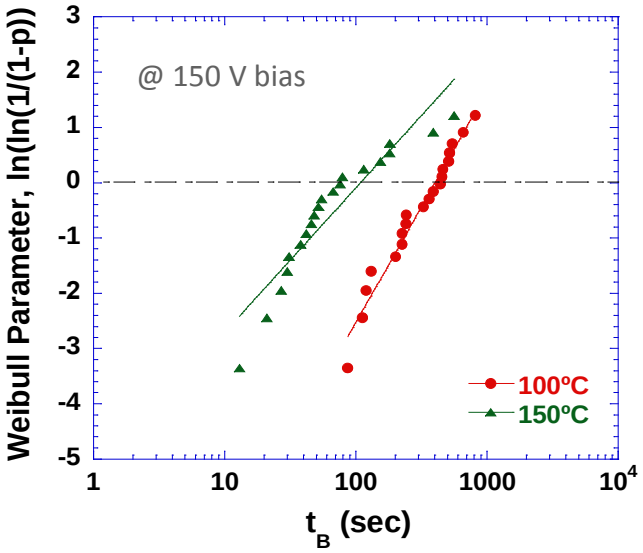


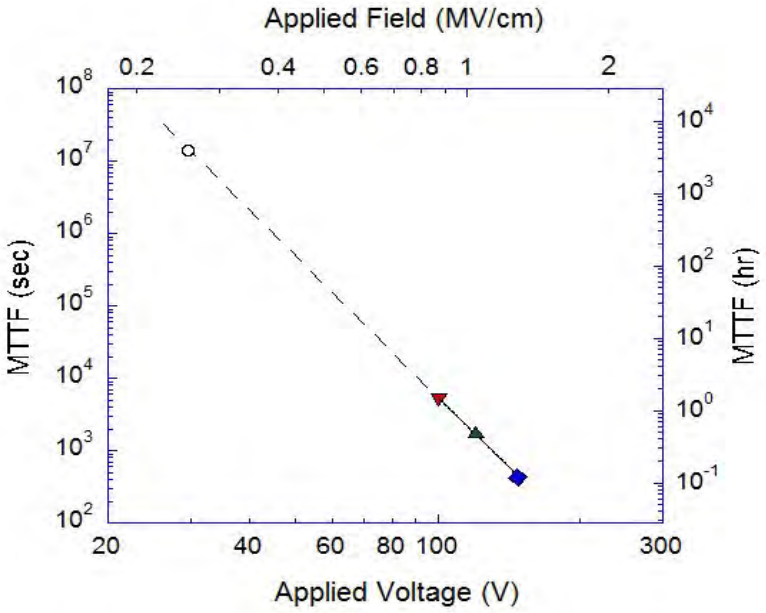


- High breakdown strength; low loss under bias field at 150°C
- Results are comparable to 2MOE processed samples; needs optimization

HALT Analysis on PLZT/LNO/Ni Films





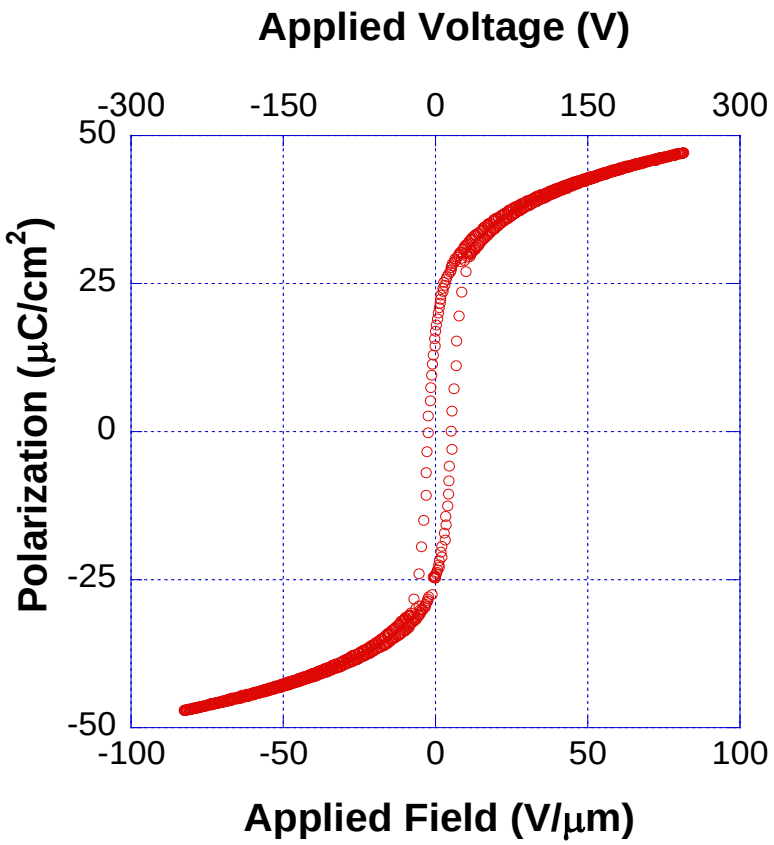


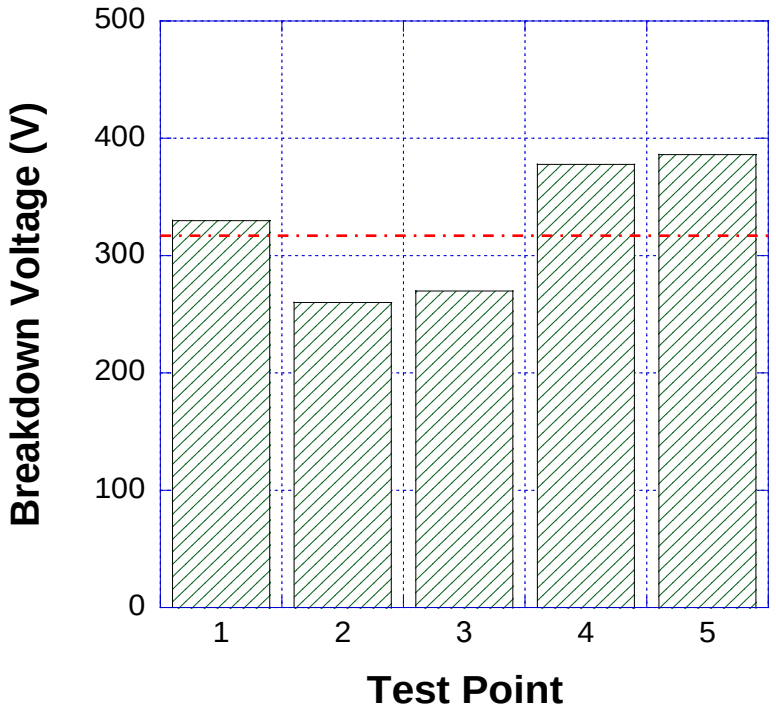
$$t = C \cdot V^{N} \exp\left(\frac{E_a}{k_B \cdot T}\right)$$

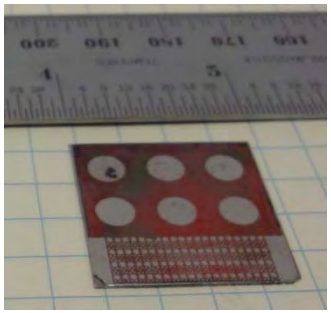
- **Lifetime estimated by measuring time to failure vs. applied voltage as function of temperature.**
- **Mean time-to-failure (MTF), voltage acceleration factor (N), and activation energy (E_a) are obtained from reliability measurement.**

Properties of 5-mm-dia. PLZT/LNO/Ni Capacitors

≈3-μm-thick film



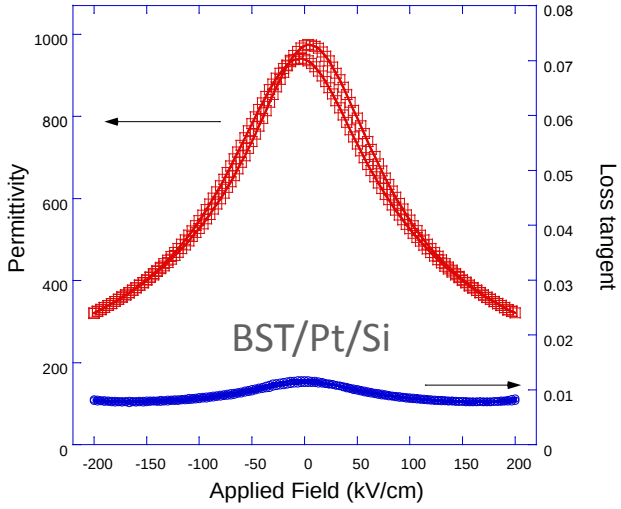


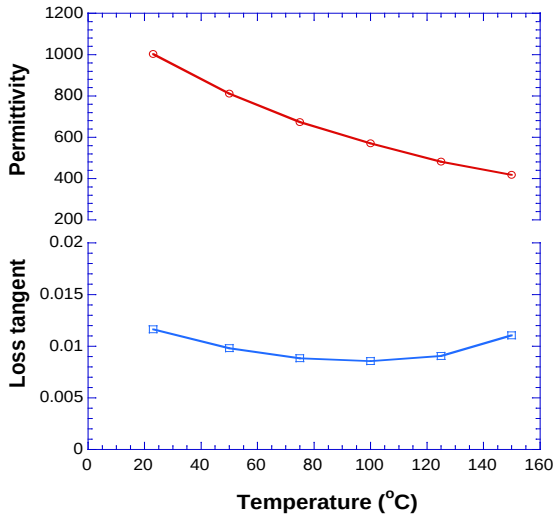


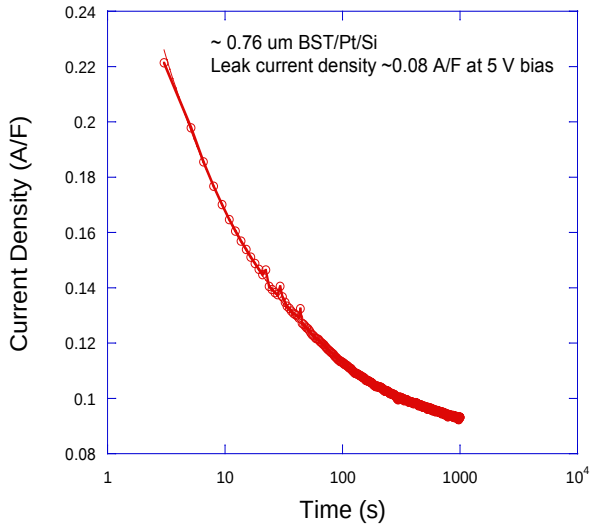
Breakdown voltages for the 5-mm caps are: 330V, 260V, 270V, 378V, 386V (Average ≈325V)

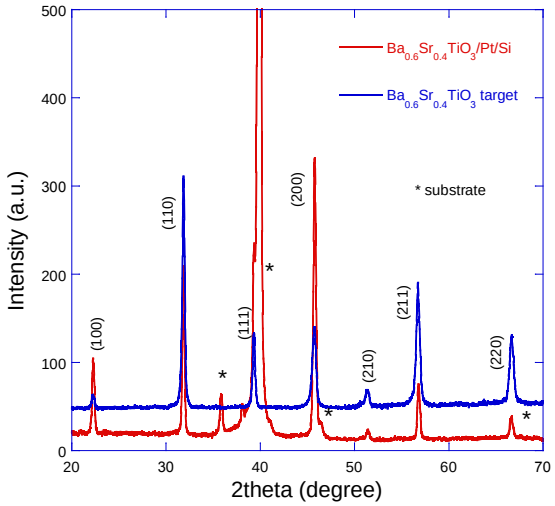
Technical Accomplishments/Results (Contd.)

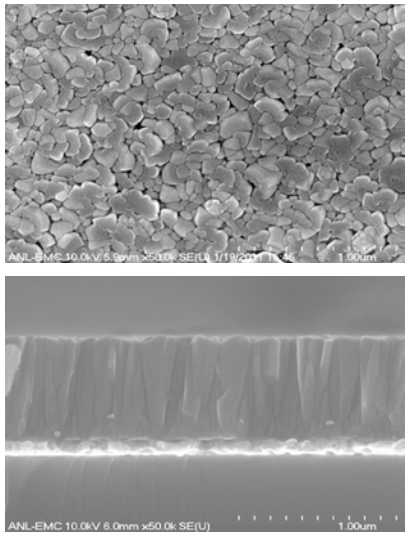
(PLD for super-structure dielectric films to improve E_b)











- Leakage ≈8 x 10^{-8} A/μF at RT
- Phase-pure, high-density film deposited by PLD