# Environmental Effects on Power Electronic Devices

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**2010 Vehicle Technologies Annual Merit Review and Peer Evaluation Meeting**
**Washington, DC**
**10 June 2010**

**Project ID #: pm017**

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# Overview

## Timeline

- Project start: October 2007
- Project end: September 2010
- Percent complete: 92%

## Budget

- Total project funding
  - DOE 100%
- FY08: $200k
- FY09: $200k
- FY10: $200k ($135k recvd as of 01Apr10)

## Barriers*

- Barriers Addressed
  - Insulated gate bipolar transistors (IGBTs) are temperature limited
  - Accurate life prediction not available
  - Power electronic devices (PEDs) not sufficient rugged
  - PEDs need improved thermal management
- Targets:
  - DOE VTP** 2015 target: 105°C Coolant
  - DOE VTP** 2015 target: 12 kW/liter

## Partners

- NTRC***/ORNL
- Powerex
- Cree

* FCVT Multi-Year Program Plan
** VTP = Vehicle Technology Program
*** NTRC = National Transportation Research Center

# Objectives

- Understand the complex relationship between environment (e.g., temperature, humidity, and vibration) and automotive power electronic device (PED) performance through materials characterization and modeling.

- Identify alternative materials and architectures internal to PEDs, and more appropriately consider mechanical properties, to improve reliability and enable higher temperature operation.

# Milestones

- **FY09: Compare cooling efficiencies in a hybrid inverter IGBT that contains contemporary and alternative ceramics within direct bonded copper (DBC) substrates.**

- **FY10: Develop a test coupon, method, and model that will estimate and measure the apparent thermal diffusivity of a PED's die-solder-DBC substrate.**

# Technical Approach

- **Develop alternative means of thermal management of PEDs.**
- **Mechanically evaluate the strength of (brittle) semiconductor chips and apply Weibull distribution statistics.**
- **Evaluate the thermal management effectiveness of PEDs and seek means to achieve improvements that will enable reliability improvement and higher temperature usage.**

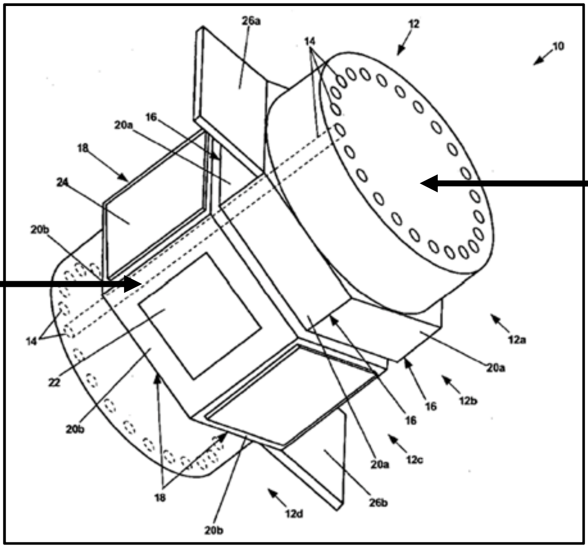
# Technical Accomplishments – 1 of 8

## *Overview of FY09 results*

- **Direct-Cooled ceramic substrate**
- **Silicon (Si) and silicon carbide (SiC) semiconductor strength: edges matter a lot**
- **Start of flash diffusivity analysis of multilaminates**

# Technical Accomplishments – 2 of 8

## *Direct-Cooled Ceramic Substrate*

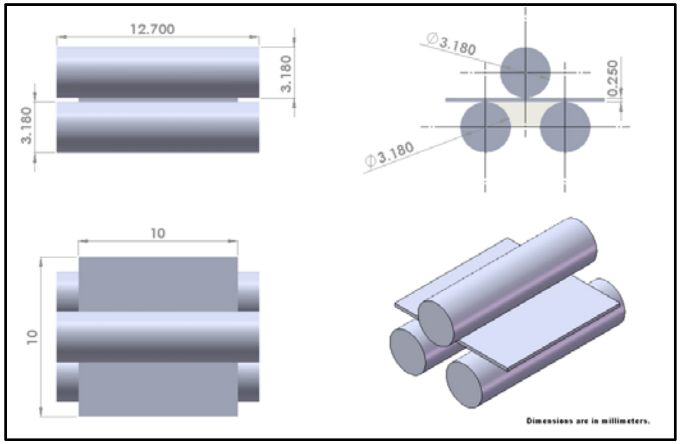



- **Patent 2009/0231812**
- **Collaboration with NTRC/ORNL's R. Wiles, K. Lowe, and C. Ayers**
- **Thermomechanical and probabilistic design assistance provided**

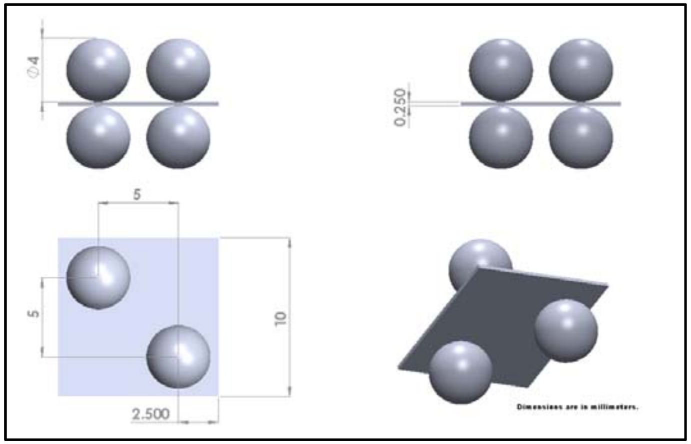
# Technical Accomplishments – 3 of 8

## *Si and SiC Semiconductor Strength: Test Methods*

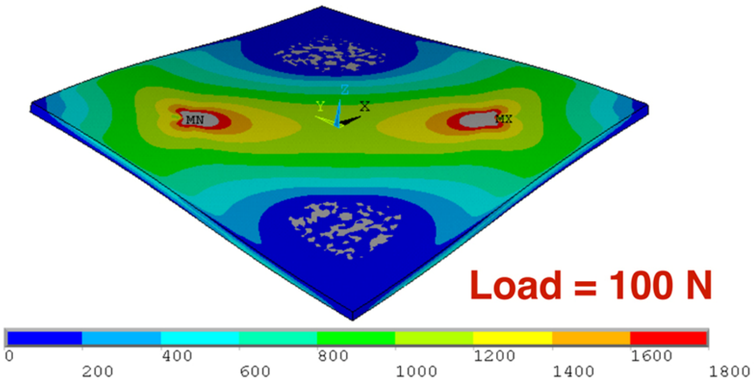
**3-Point-Bending**




**Anticlastic Bending**



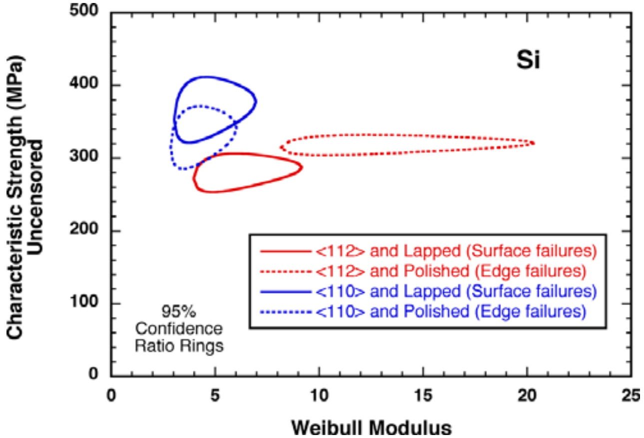

**Induced Stress and Displacement Profiles of Anticlastic Bending**



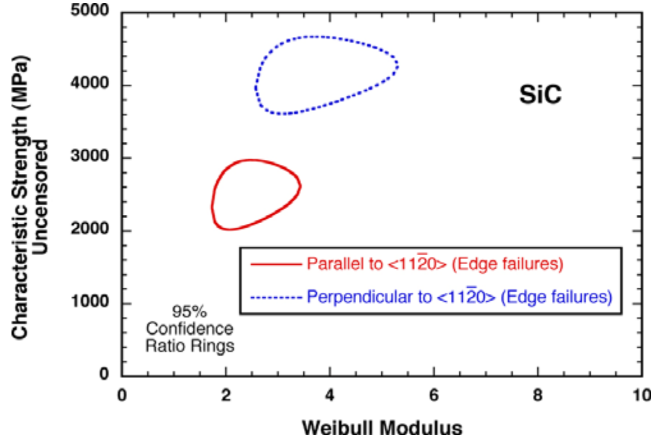
# Technical Accomplishments – 4 of 8

## *3-Point and Anticlastic Bend Strength Results*

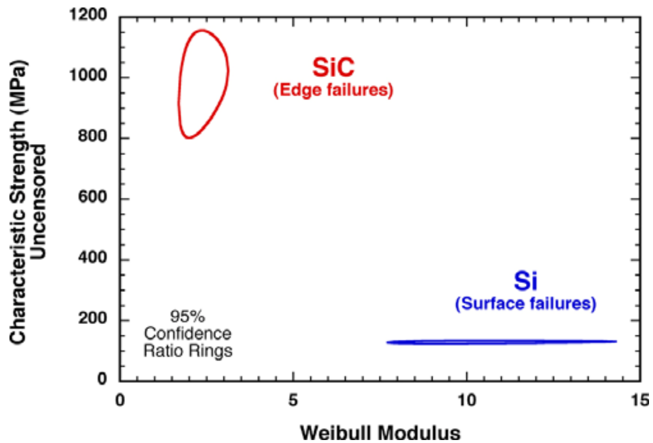
### 3-Pt-Bending




### 3-Pt-Bending



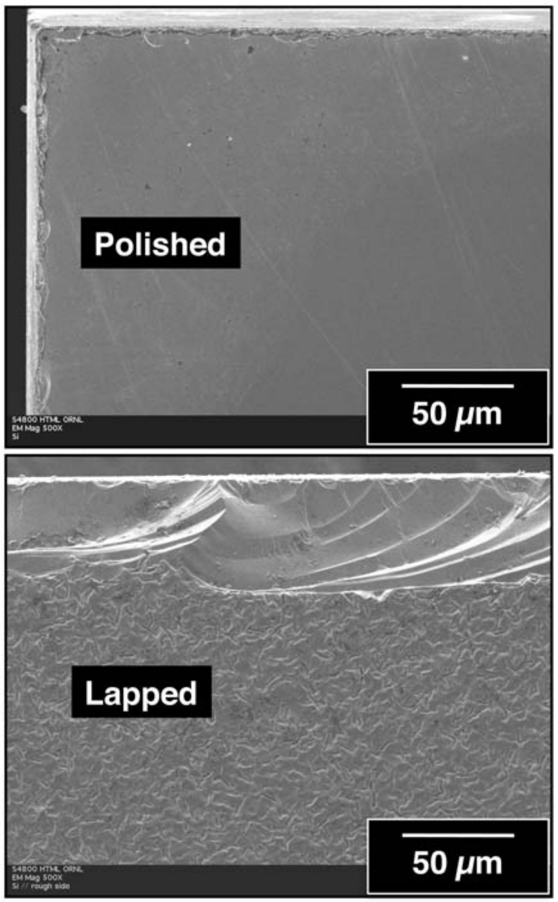

### Anticlastic Bending



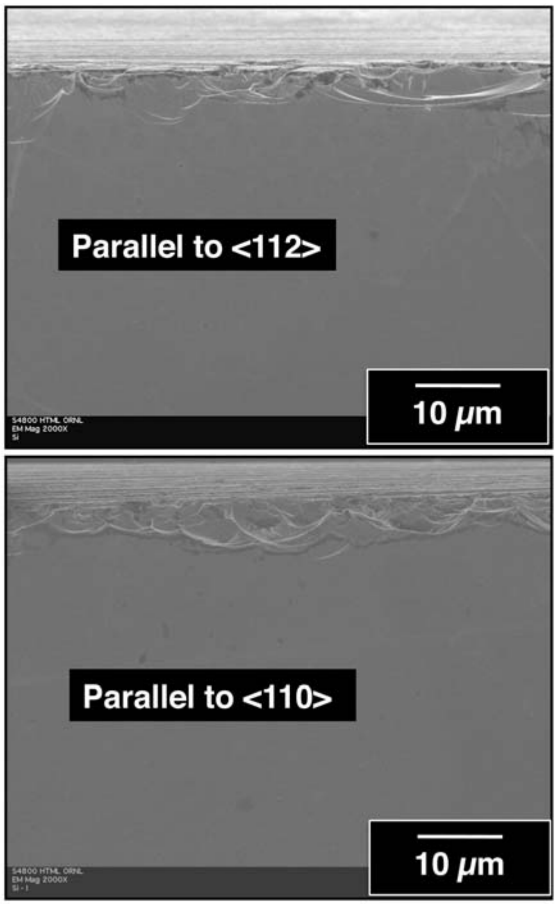
# Technical Accomplishments – 5 of 8

## *Edge Quality and Chipping Affects Failure Stress*

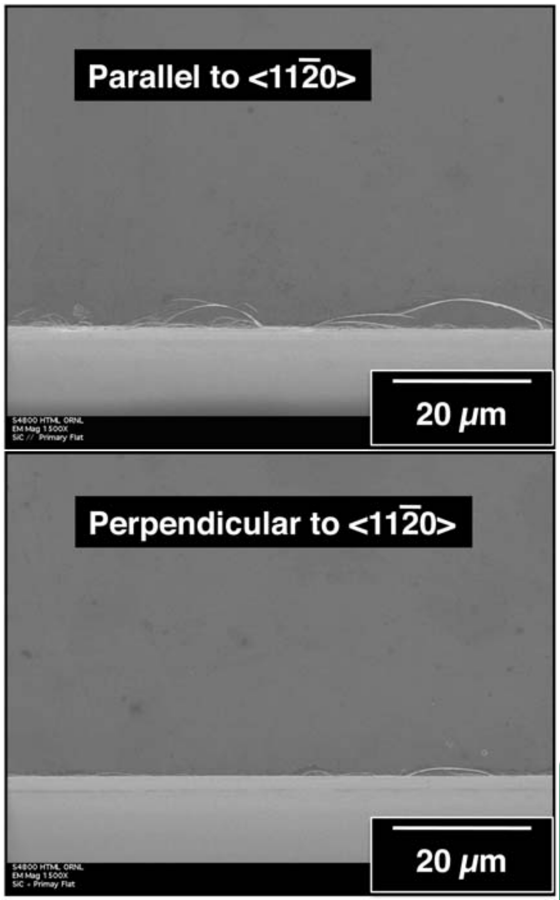
**Silicon**




**Silicon**

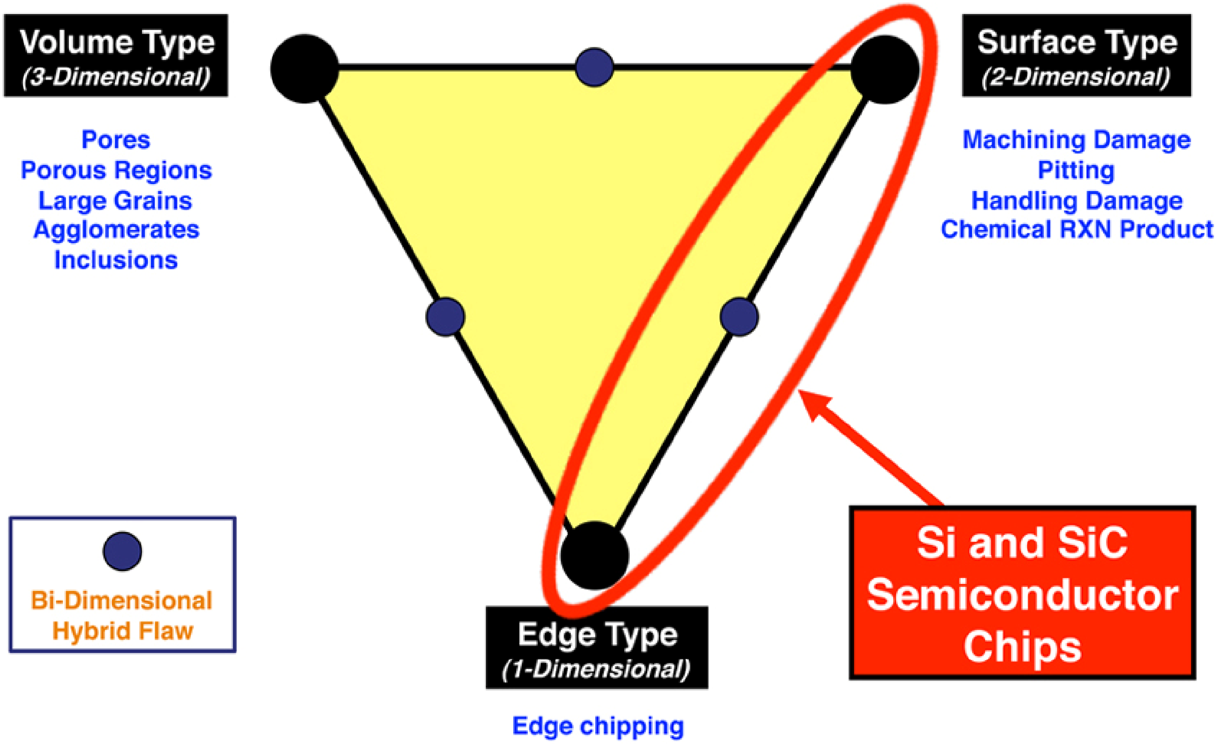



**Silicon Carbide**



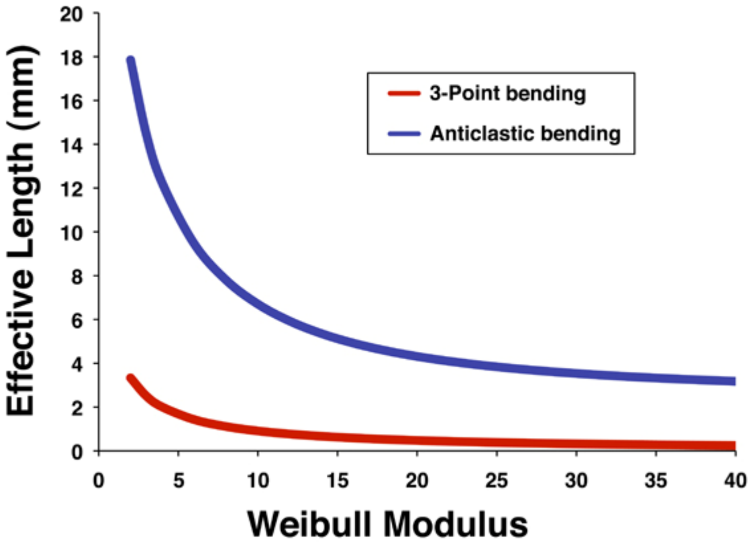
# Technical Accomplishments – 6 of 8

## *Strength-Limiting Flaw Types in Semiconductor Dies*



# Technical Accomplishments – 7 of 8

## *Strength-Size-Scaling*




**Weibull distribution (length)**

$$P_f = 1 - \exp\left[-\left(\frac{\sigma_{\max}}{\sigma_{0L}}\right)^m L_e\right]$$

**Size-scaling among lengths**

$$\left(\frac{\sigma_{f1}}{\sigma_{f2}}\right) = \left(\frac{L_{e2}}{L_{e1}}\right)^{\frac{1}{m}}$$

# Technical Accomplishments – 8 of 8

## *Apparent Thermal Diffusivity of Multilaminates*

- Use flash diffusivity with power electronic architecture
- Marry experiment with transient finite element analysis
- Estimate apparent thermal diffusivity
- Interpret interfacial thermal losses

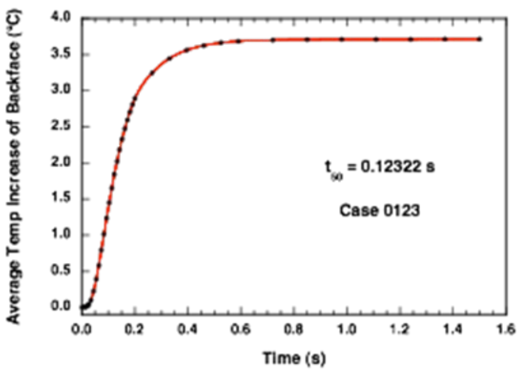
$$D = \frac{\kappa}{\rho \bullet Cp}$$

D = diffusivity
$\kappa$ = thermal conductivity
$\rho$ = density
Cp = heat capacity

$$D = \frac{0.1388 \bullet T^2}{t_{50}}$$

D = diffusivity
T = thickness
$t_{50}$ = time to reach 50% max temp

FEA predicted response & then correlate to experimental response



# Future Work

**Project ends in FY10**

# Summary

- **A direct-cooled ceramic substrate was developed as an alternative means of thermal management of power electronic devices.**

- **The strength of Si and SiC semiconductor chips were measured and related to Weibull distributions and strength-size-scaling.**

- **Apparent thermal diffusivity analysis of power electronic device multilaminate structures has been initiated.**