Electro-thermal-mechanical Simulation and Reliability for Plug-in Vehicle Converters and Inverters

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Project ID # APE 026

Azure Dynamics

Overview

Timeline

- October 2009
- October 2012
- 50% Complete

Budget

- Total project funding
  - $400K
- Funding received FY09
  - $ 100K
- Funding received FY10
  - $ 100K
- Funding expected FY11
  - $ 200K

Barriers

Need electro-thermal-mechanical modeling, characterization, and simulation of advanced technologies to:

- Improve electrical efficiency
- Improve package thermal performance and increase reliability
- Reduce converter cost

Partners

- NIST- Electro-thermal modeling
- UMD/CALCE – Reliability modeling
- VTech – Soft switching module
- Delphi – High current density module
- NREL – Cooling technology
- Azure Dynamics – System Integration

Azure Dynamics

Relevance of the Study

Objective: Provide theoretical foundation, measurement methods, data, and simulation models necessary to optimize power module electrical, thermal, and reliability performance for Plug-in Vehicle inverters and converters.

For FY 11:

1) Utilize electro-thermal-mechanical models to simulate VTech Soft Switching module performance (electrical, thermal, package life)
2) Utilize electro-thermal models to simulate Delphi's Viper module performance (high current IGBT SOA, package life)
3) Coordinate with NREL to identify relevant inverter cooling systems and develop thermal network component models for them
4) Complete physics of failure models and develop method to include them in electro-thermal-mechanical simulation

Milestones/Decision Points

Month/Year	Milestone or Go/No-Go Decision
June 11	Milestone: 1a) Evaluate trade-offs for different semiconductor component selections in VTech module
Oct. 11	Milestone: 1b) Evaluate thermal stresses at module interfaces for VTech module
Dec. 11	Milestone: 1c) Use physics of failure models to evaluate impact on VTech module life
Aug.11	Milestone: 2a) Simulate fault conditions to determine safe operating area of IGBT in high current density Viper module
Nov. 11	Milestone: 2b) Evaluate thermal stresses in Viper module for nominal and fault operating conditions
May 11	Milestone: 3a) With NREL, Identify representative cooling system configurations (liquid-, air-cooled, etc.)
Dec. 11	Milestone: 3b) Determine thermal-network-component model parameters for representative cooling systems
Oct. 11	Milestone: 4a) Perform thermal cycling degradation and monitoring on DBC stack for range of conditions (initial-T, ΔT, T-ramp-rate) necessary to calibrate degradation model
Dec. 11	Milestone: 4b) Devise methodologies to utilize electro-thermal-mechanical simulations with physics-of-failure models to calculate lifetime prediction for modules in vehicles

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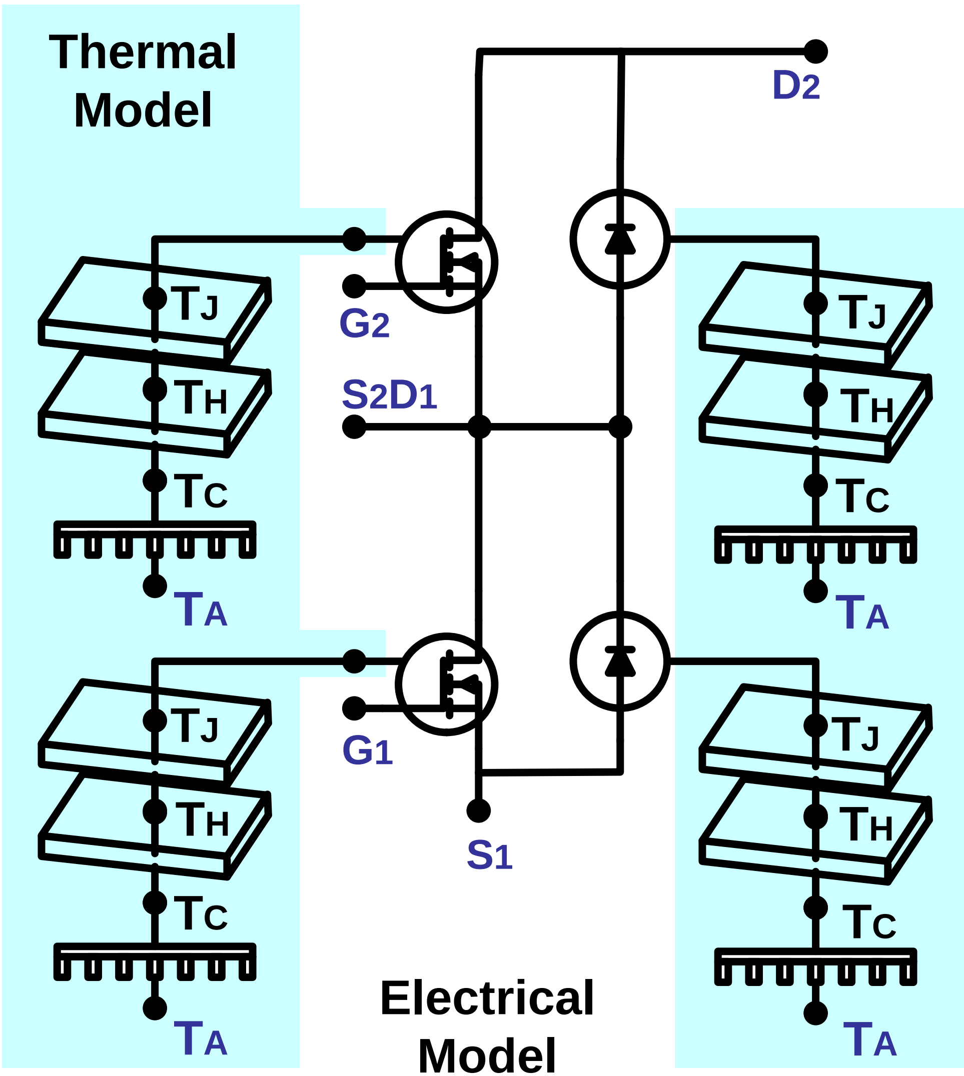
Approach:
Measurement, Modeling, and Simulation

- Develop dynamic electro-thermal Saber models, perform parameter extractions, and demonstrate validity of models for:
  - Silicon IGBTs and PiN Diodes
  - Silicon MOSFETs and CoolMOSFETs
  - SiC Junction Barrier Schottky (JBS) Diodes

- Develop thermal network component models and validate models using transient thermal imaging (TTI) and high speed temperature sensitive parameter (TSP) measurement.

- Develop thermal-mechanical degradation models and extract model parameters using accelerated stress and monitoring:
  - Stress types include thermal cycling, thermal shock, power cycling
  - Degradation monitoring includes TTI, TSP, X-Ray, C-SAM, etc.

Approach: Electro-Thermal Simulation



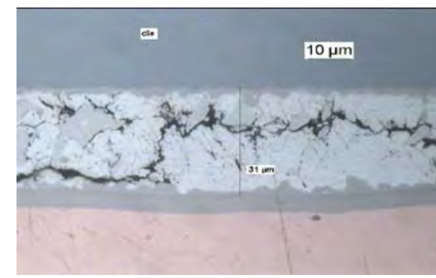
- Electro-thermal semiconductor models
  - Si IGBTs
  - Si MOSFETs and CoolMOS
  - Si PiN and SiC JBS Diodes
- Thermal network component models
  - Die
  - Die Attach
  - DBC Layers
  - Baseplate
  - Cooling system
- The power dissipation in electrical components provides heat to the thermal network.
- Thermal network component models are validated using NIST high speed transient thermal imaging (TTI) and high speed temperature sensitive parameter (TSP) measurements.

Approach: Power Module Thermo-Mechanical Degradation Mechanisms

- Wirebonds – primary failure site for power cycling
  - Wire flexure fatigue

$$\varepsilon = \frac{(R-\rho_f)d\psi}{\rho_i\psi_i} \approx \frac{(\bar{r}-\rho_f)d\psi}{\rho_i\psi_i} = \frac{r(\psi_i-\psi_f)}{\rho_i\psi_i} = r(\kappa_i-\kappa_f) \quad [1]$$

- Die attach –primary failure site for narrow temperature range thermal cycling
  - Attach fracture and fatigue

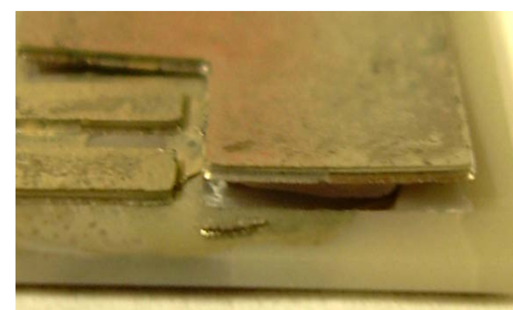


[2]

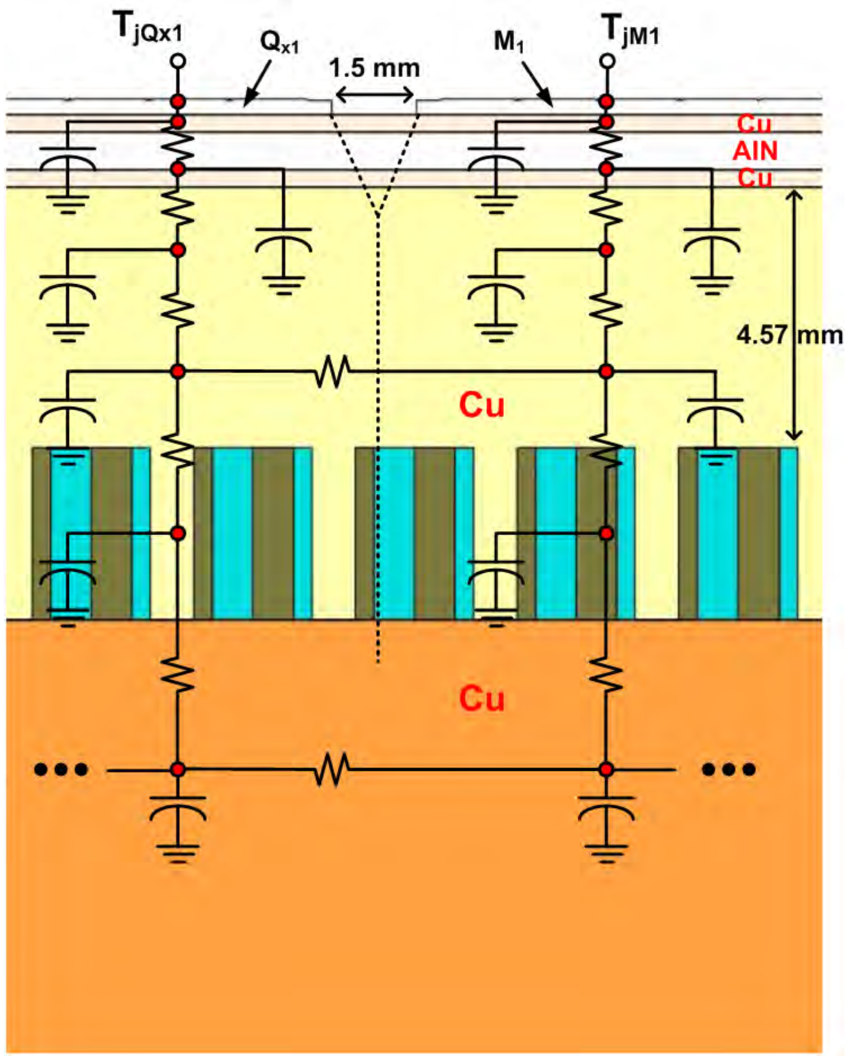
$$Energy = U_e + W_p + W_c = U_{e0}N_{fe}^{b} + W_{p0}N_{fp}^{c} + W_{c0}N_{fc}^{d}$$

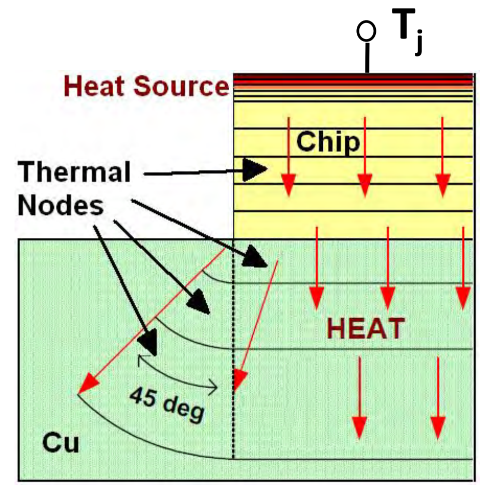
- Substrate – primary failure site for wide temperature range thermal cycling
  - Substrate fracture and fatigue
  - Copper delamination

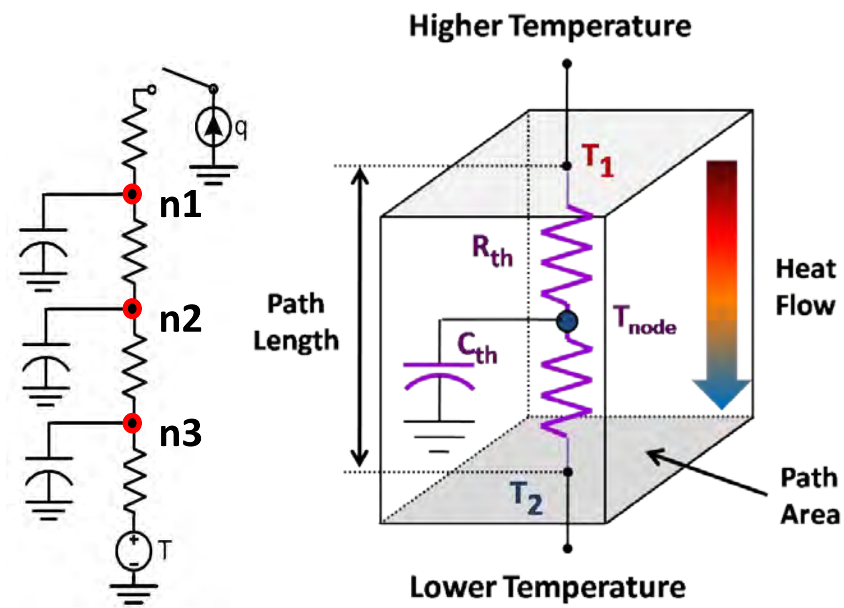
$$\frac{da}{dN} = A(\Delta K)^n$$



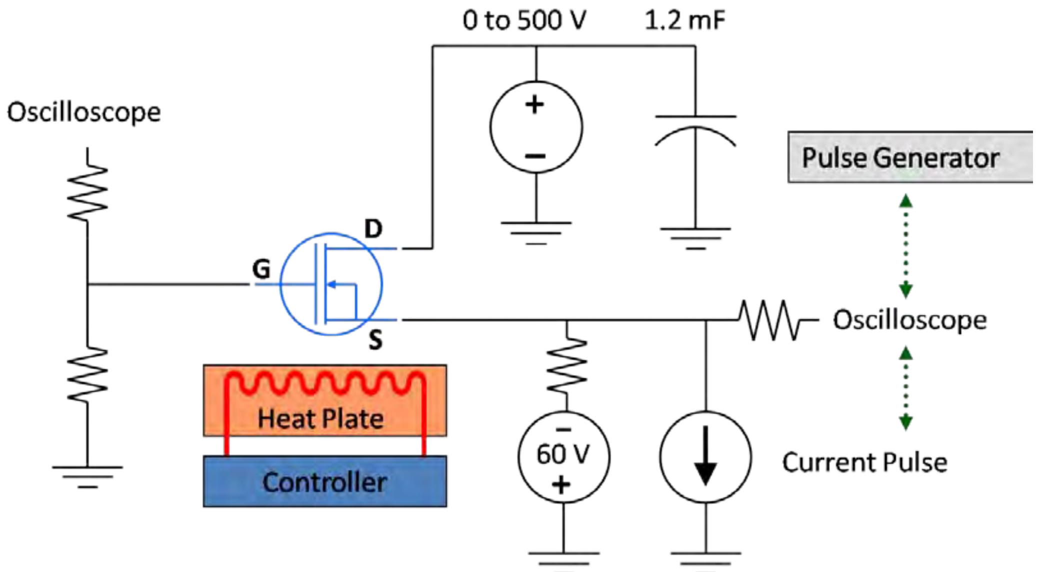
Method: Thermal Network Component Models

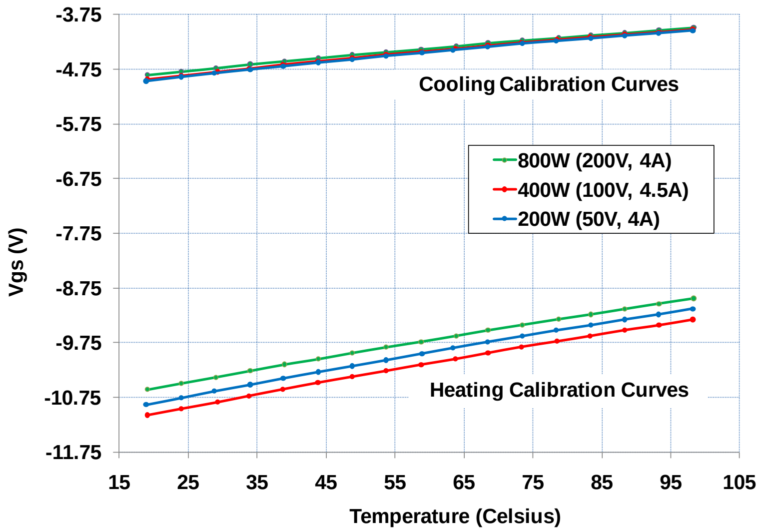


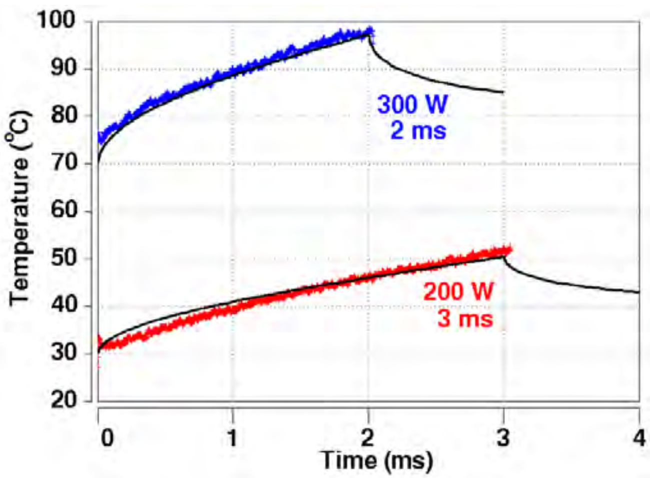


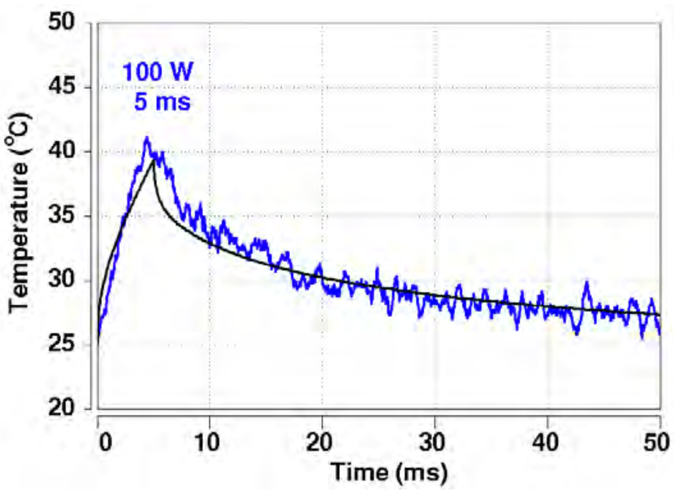


Method: High-Speed Temperature Sensitive Parameter (TSP) Measurement

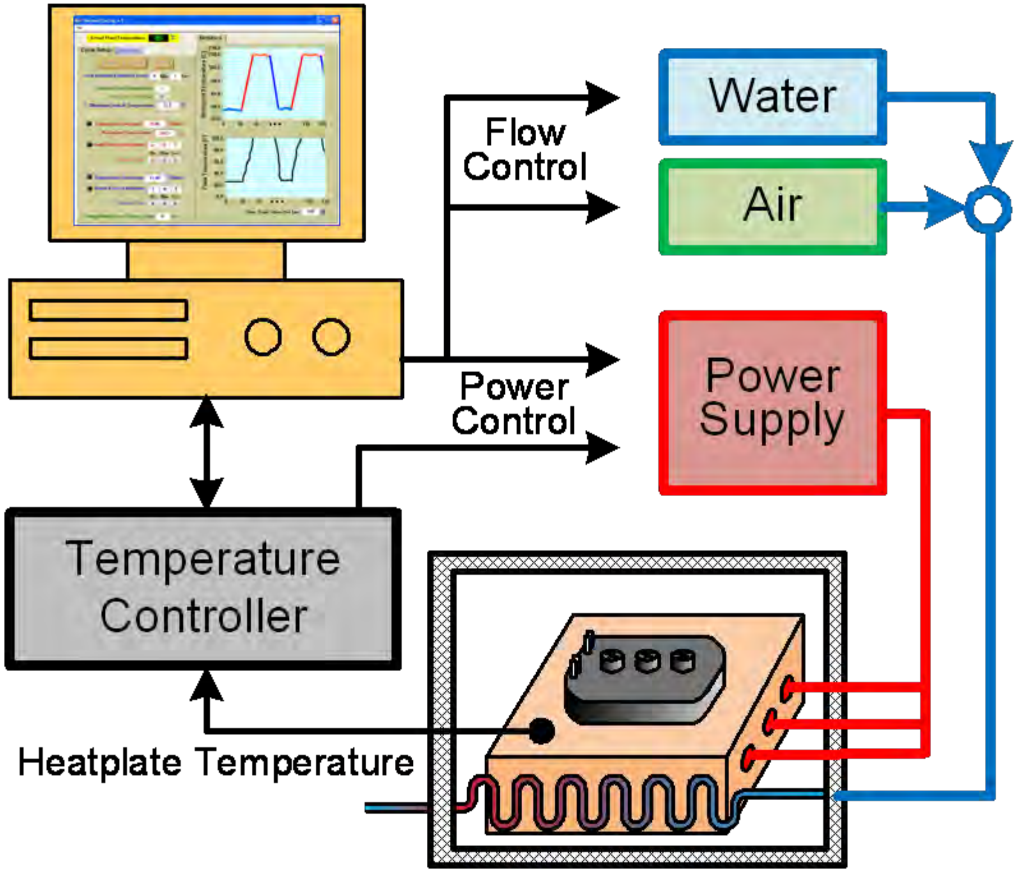








Method: High-Speed Thermal Cycling/Shock (T-initial, ΔT, T-ramp-rate)

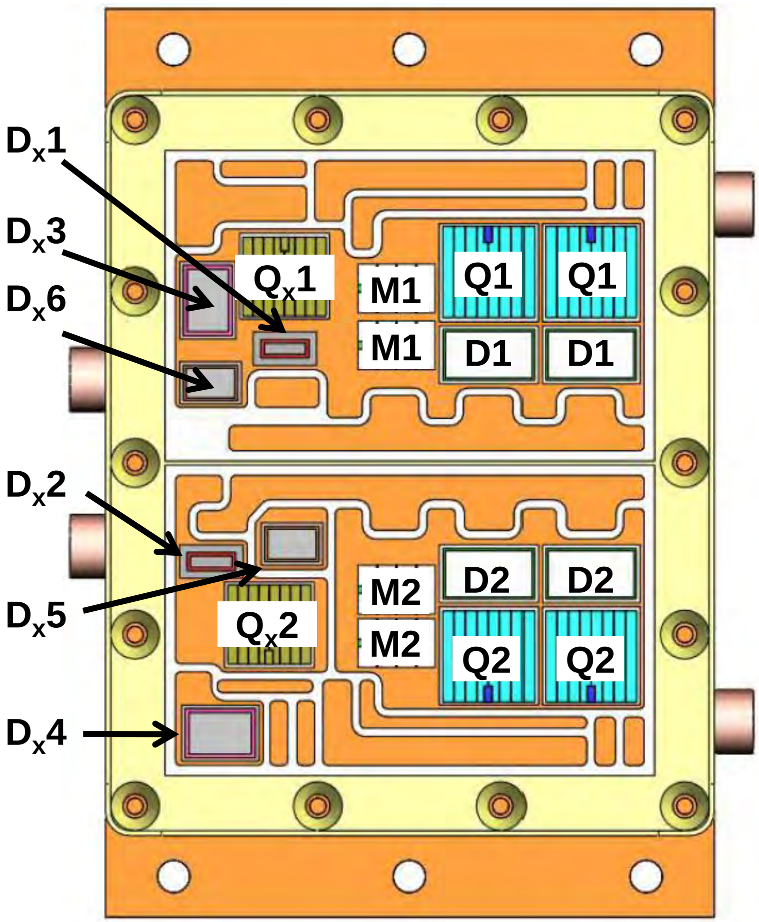


For each thermal cycle:

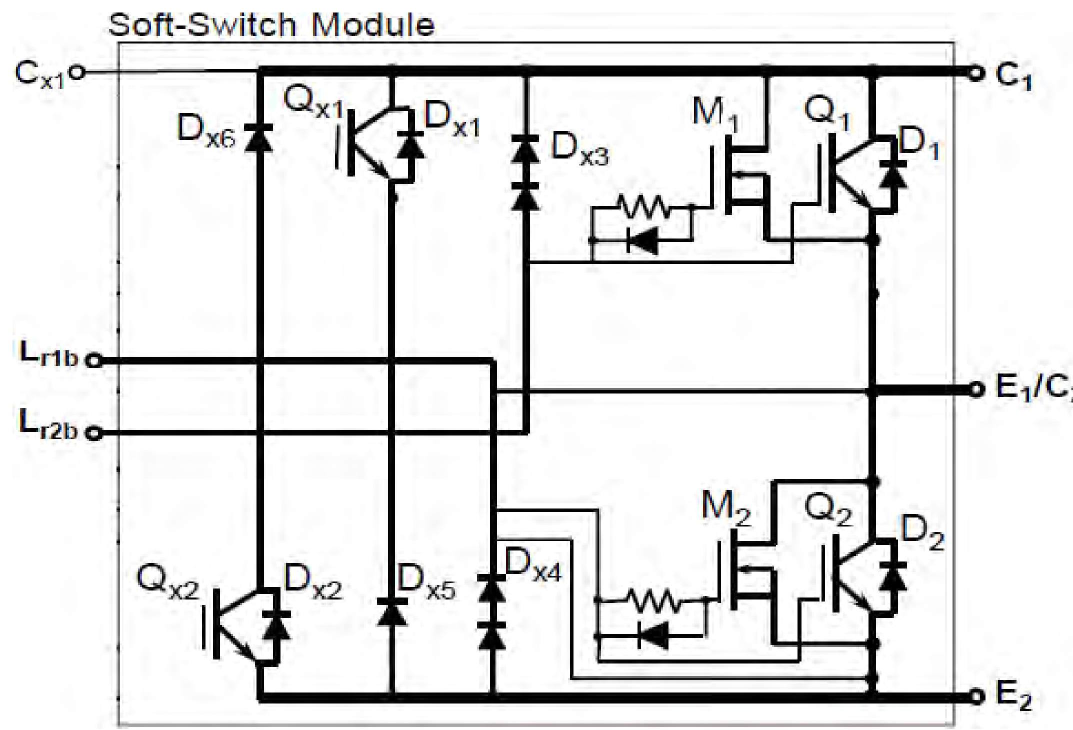
- Computer controls T-initial, ΔT, T-ramp-rate:
- Power is delivered to the heating elements in the baseplate to increase the temperature of the DUT at a user-controlled rate.
- Cycle maximum temperature is maintained for a specified dwell time.
- Air and/or water delivered to baseplate to reduce temperature at a user-controlled rate.
- Cycle minimum temperature is maintained for a specified dwell time.

Application: VTech Soft Switching Module

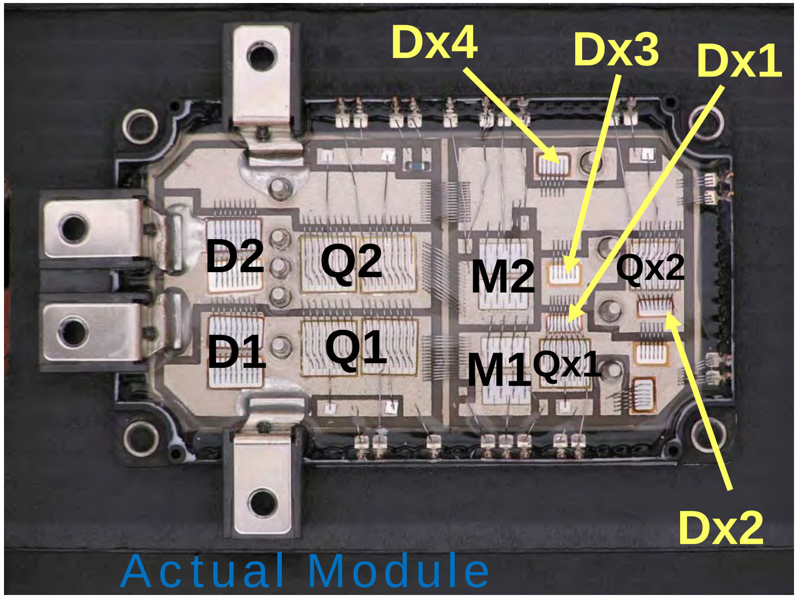
Module Schematic



Circuit Diagram



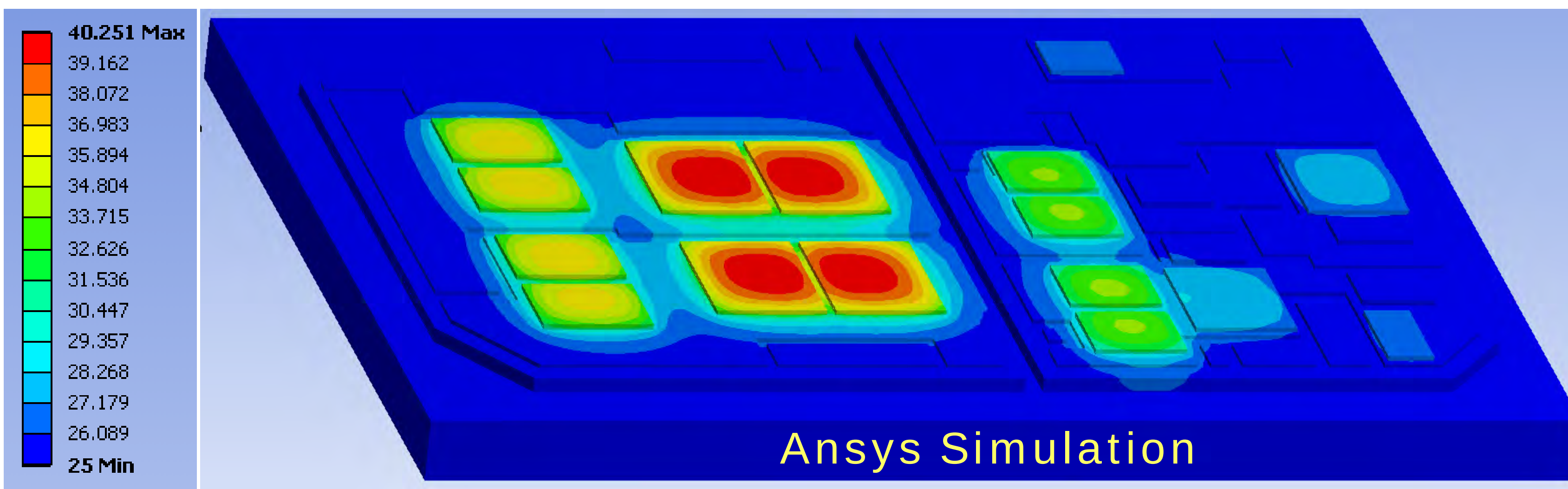
Validation: 3D Simulation of VTech Module



Module Section	Legend in the Circuit Diagram	Total Avg Power Loss/Chip (W)
Main Switch	Q1, Q2	116.0
	M1, M2	36.0
	D1, D2	58.0
Auxilary Switch	Qx1, Qx2	18.0
	Dx1, Dx2	0.5
Re-Setting Schottky Diode	Dx3, Dx4	6.5
Noise Kick Diode	Dx5, Dx6	0.5

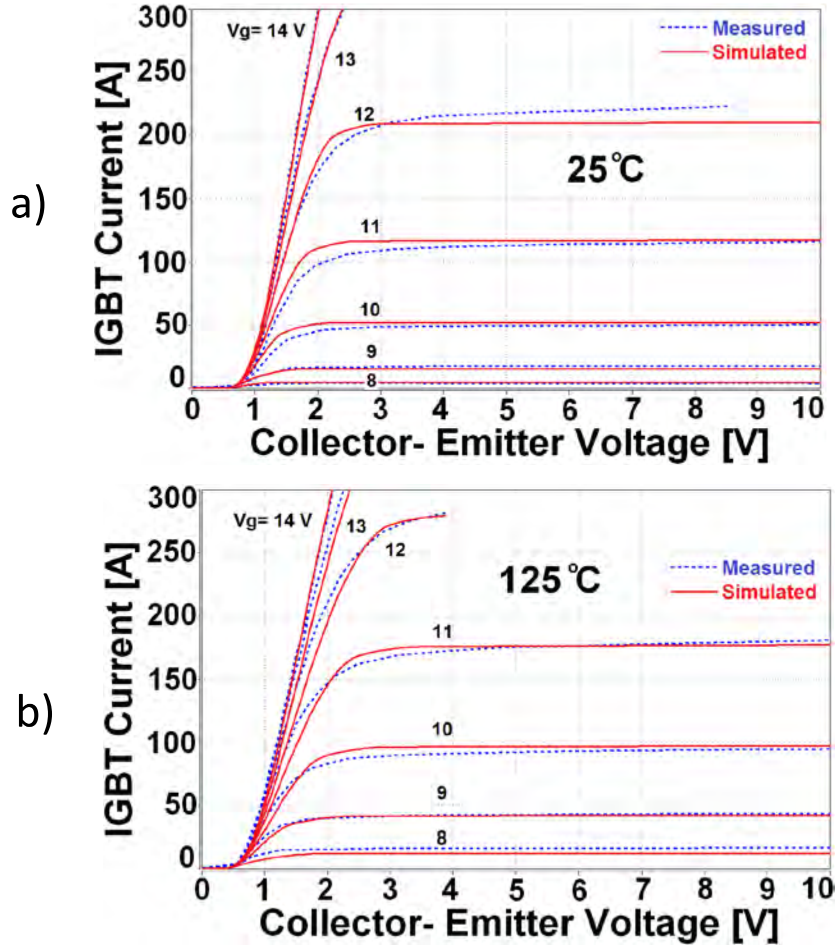
Average power losses were simulated.

Steady State Conditions @ 25°C



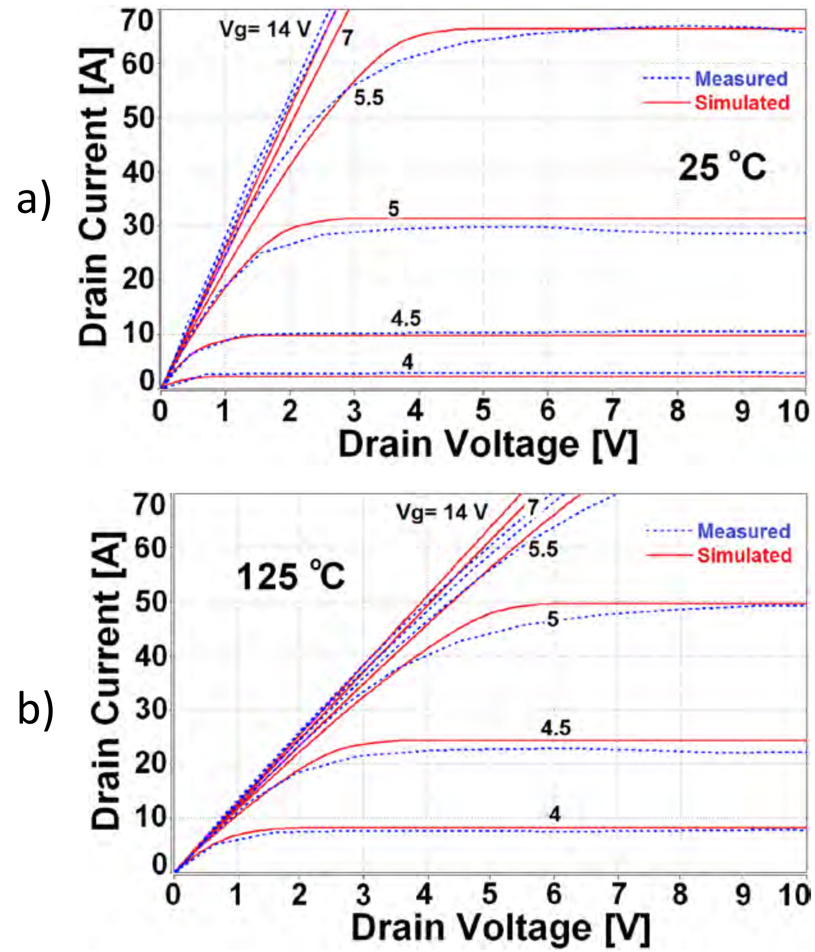
Validation: IGBT and CoolMOS Output Current

600 V, 300 A Si IGBT



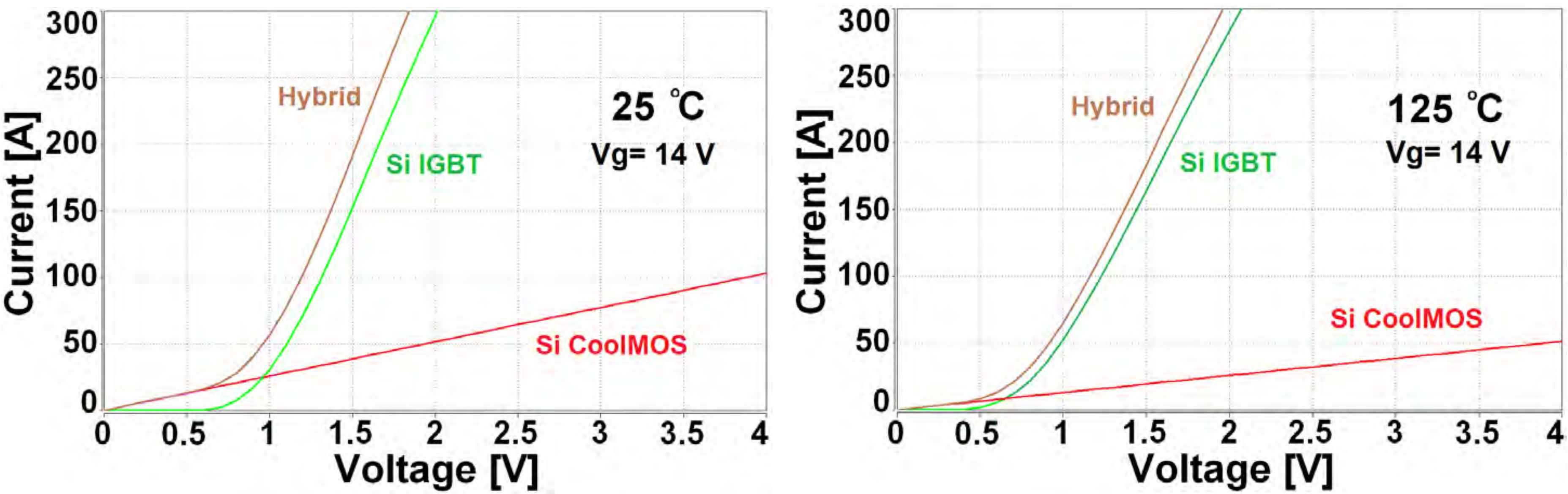
Comparison of measured (dashed) simulated (solid) output characteristics at a) 25 ^oC and b) 125 ^oC for a 600 V, 300 A Si IGBT.

650 V, 60 A Si CoolMOS



Comparison of measured (dashed) simulated (solid) output characteristics at a) 25 ^oC and b) 125 ^oC for a 650 V, 60 A Si CoolMOS.

Analysis: Paralleled Si IGBT and CoolMOS

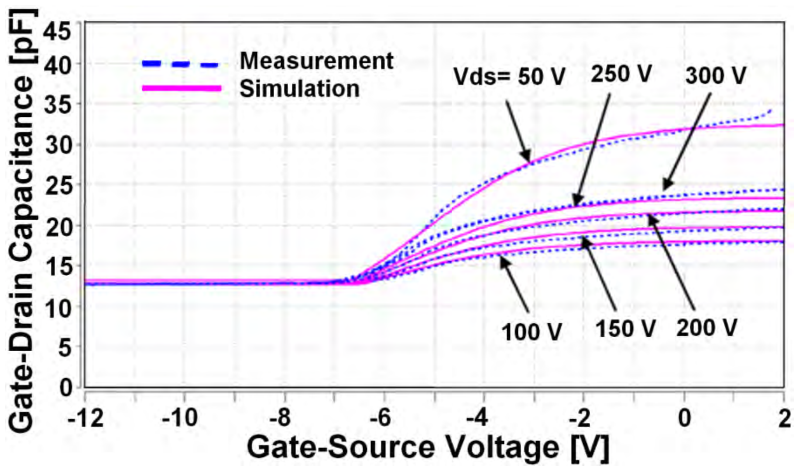


a) b)

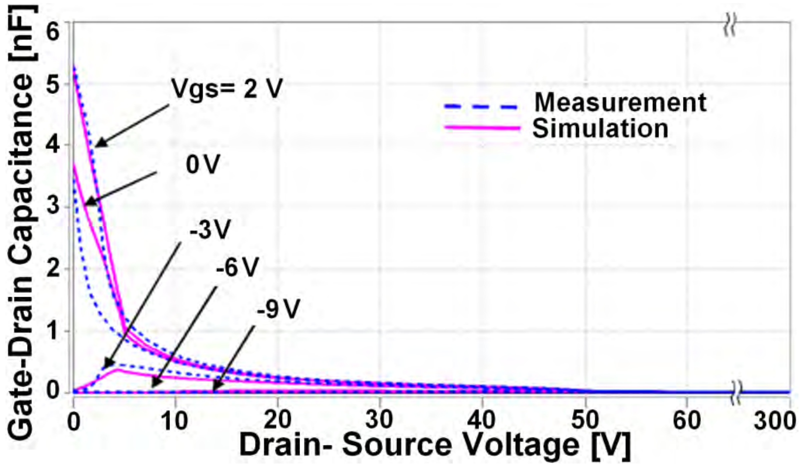
Comparison of measured (dashed) simulated (solid) output characteristics for a 600 V, 300 A Si IGBT and 650 V, 60 A Si CoolMOS at a) 25 ^{o}C and b) 125 ^{o}C.

Validation: 650 V, 60 A CoolMOS Capacitance

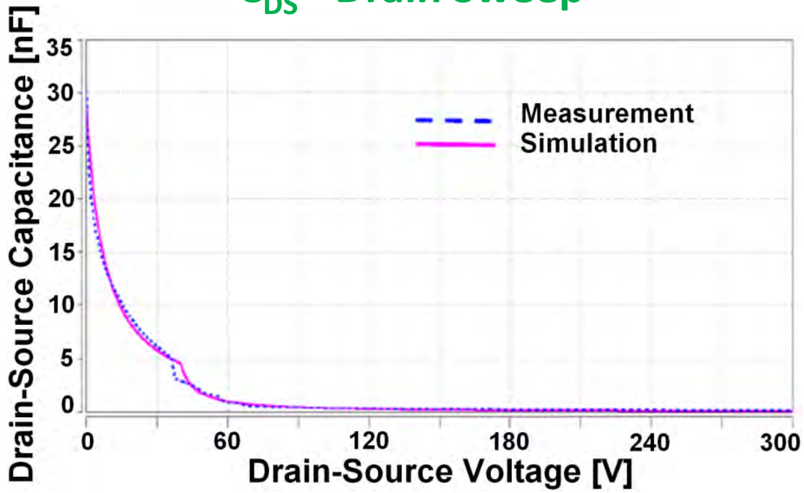
C_{GD} – Gate Sweep



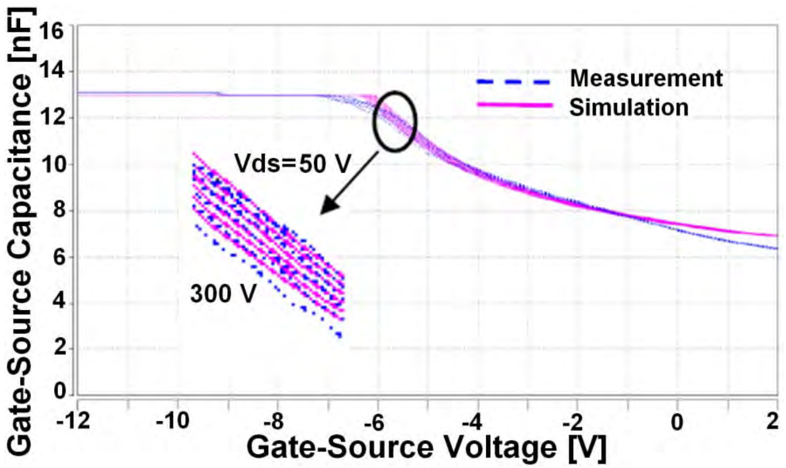
C_{GD} - Drain Sweep



C_{DS} - Drain Sweep



C_{GS} - Gate Sweep



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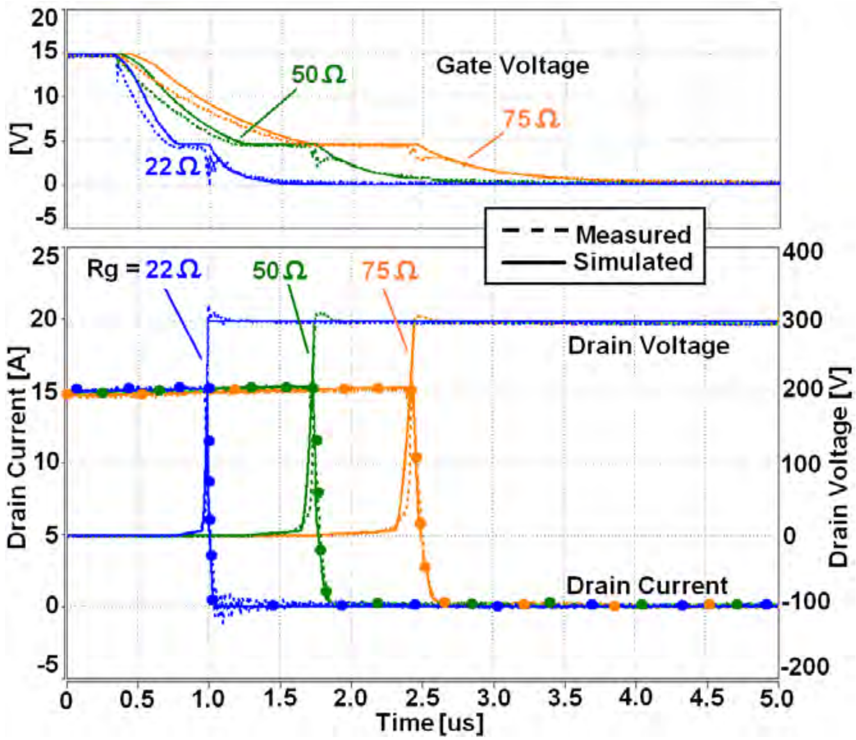
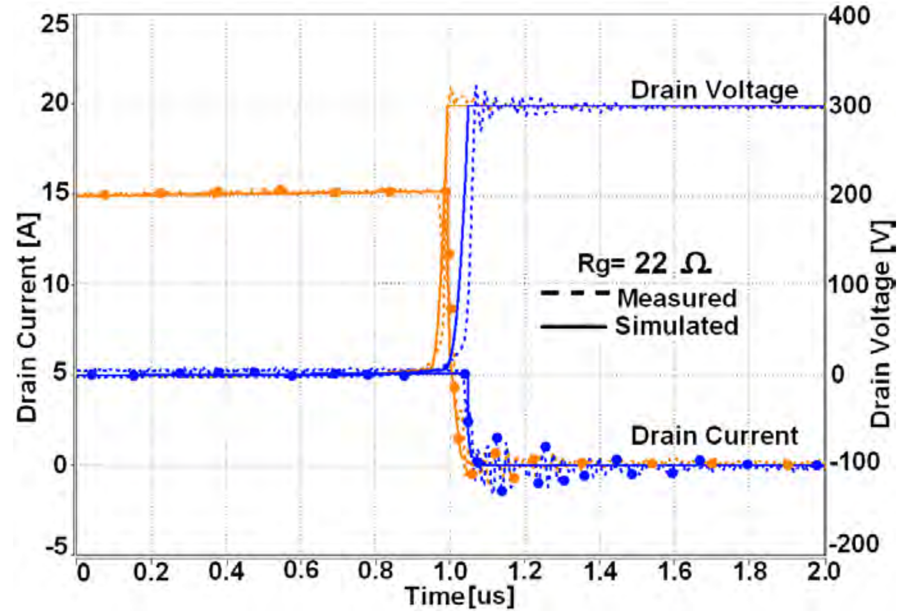
Validation: 650 V, 60 A CoolMOS for Inductive Load Turn-off

Gate Resistor Dependence



Current Dependence



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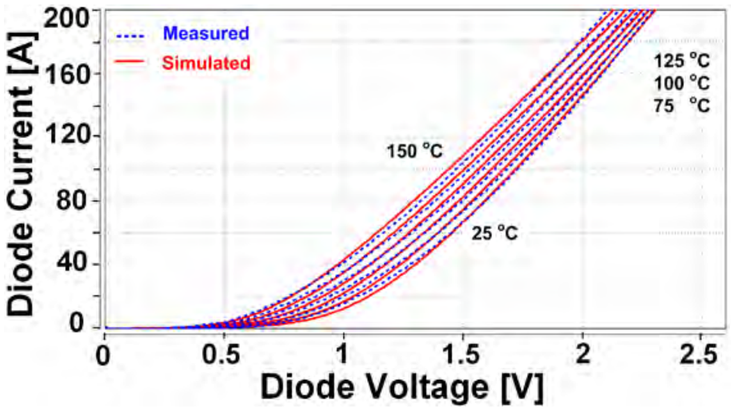
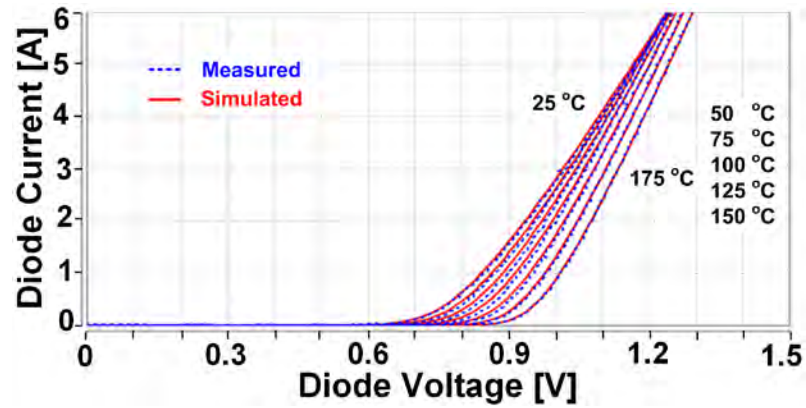
Analysis: Si PiN, SiC JBS, CoolMOS-Body Diodes

Si PiN Diode



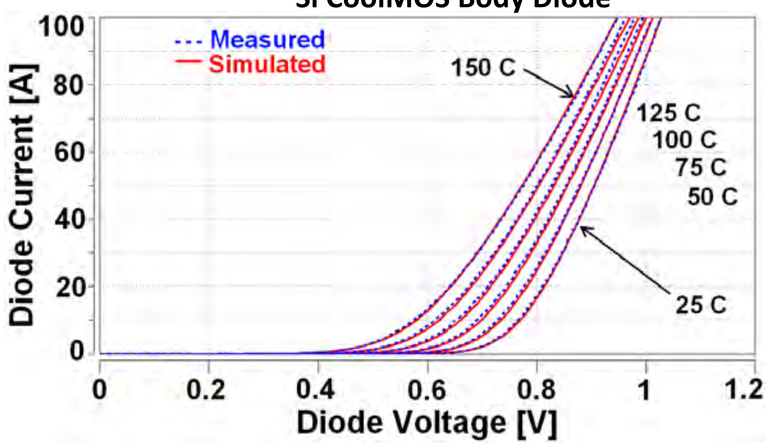
Comparison of measured (dashed) simulated (solid) output characteristics at 25 °C, 50 °C, 75 °C, 100 °C, 125 °C, and 150 °C for a 600 V, 200 A Si PiN diode.

SiC JBS Diode

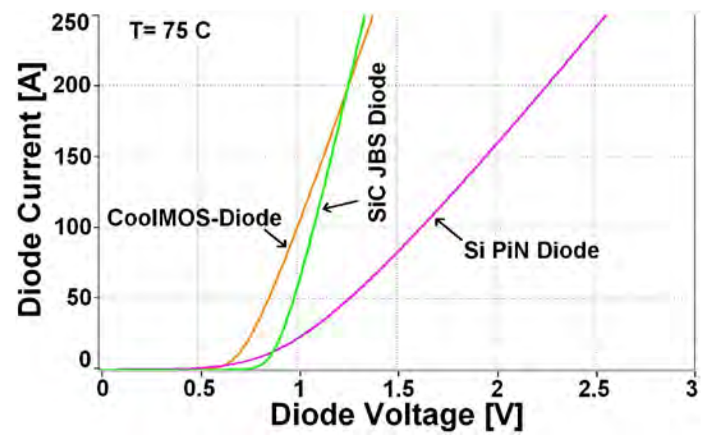


Comparison of measured (dashed) simulated (solid) output characteristics at 25 °C, 50 °C, 75 °C, 100 °C, 125 °C, 150 °C and 175 °C for a 600 V, 6 A Si PiN diode.

Si CoolMOS Body Diode

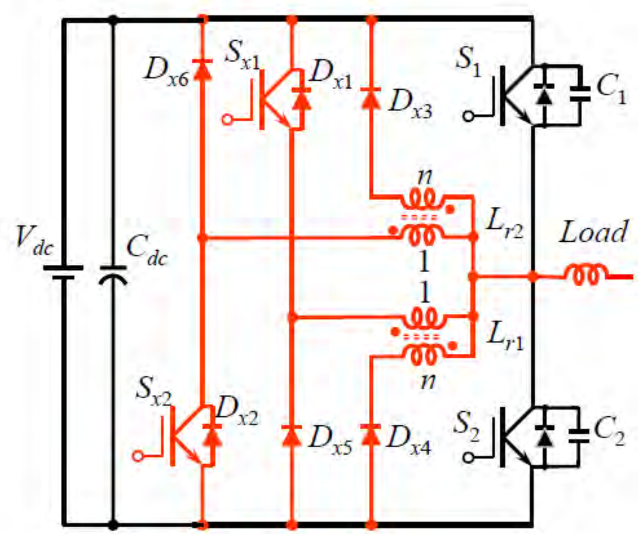


Comparison of measured (dashed) simulated (solid) output characteristics at 25 °C, 50 °C, 75 °C, 100 °C, 125 °C, 150 °C and 175 °C for the body diode of a 650 V, 60 A Si CoolMOS.

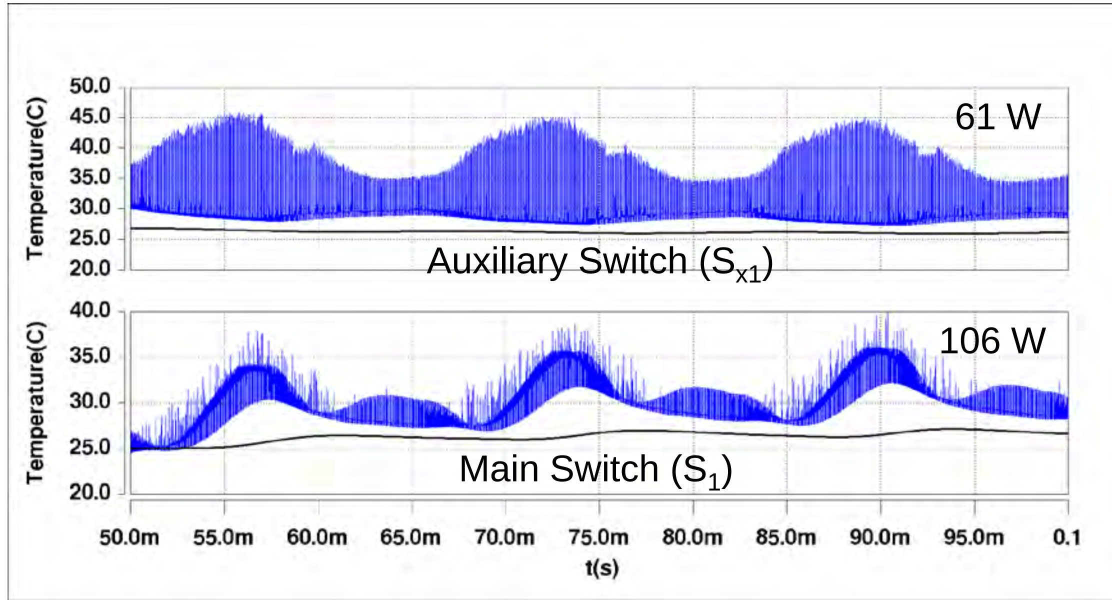


Comparison of forward characteristics for 650 V, 60 A Si CoolMOS anti-parallel diode; 600 V, 200 A SiC JBS diode; and 600 V, 200 A Si PiN diode at 75 °C.

Demonstration: Electro-thermal Simulation of Soft-Switching Vehicle Inverter



Soft Switching Inverter Topology



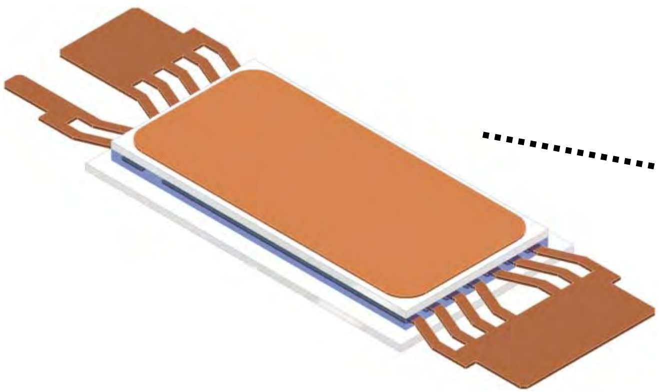
Electro-thermal simulation of junction temperature for switches undergoing half-sine wave power cycle.

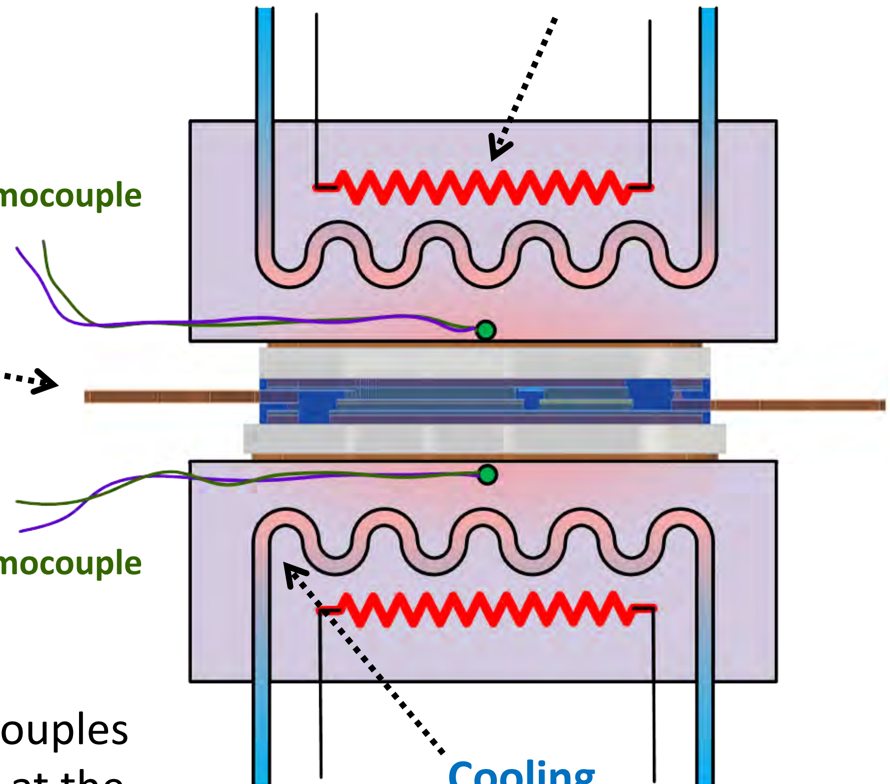
Junction temperature (**blue lines**)

Bottom of the chip temperature (**black lines**)

Application: Delphi – Viper Module Double Sided Cooling Model

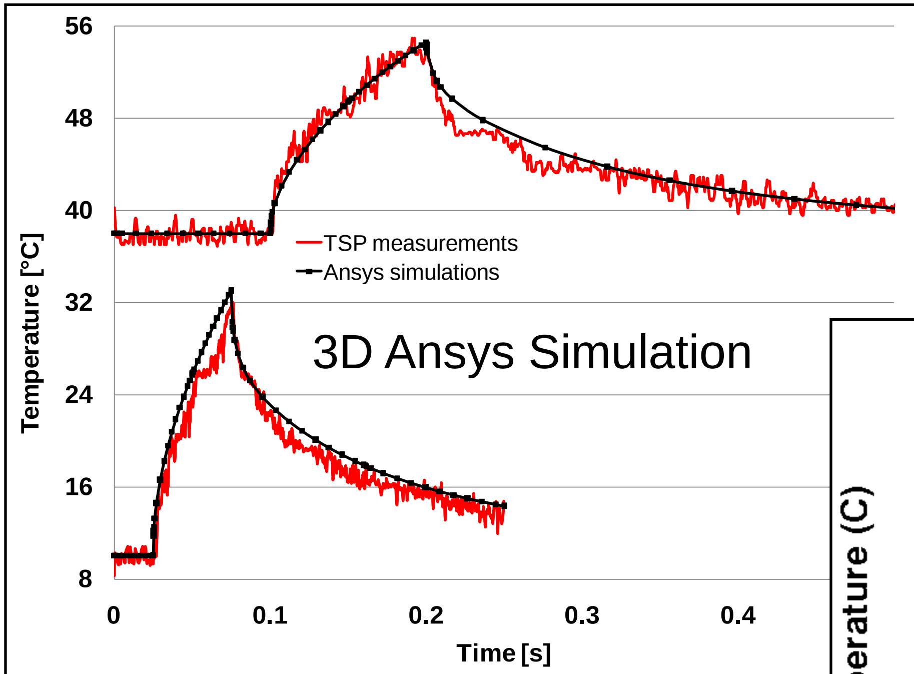
Module
(2.7 mm thick)



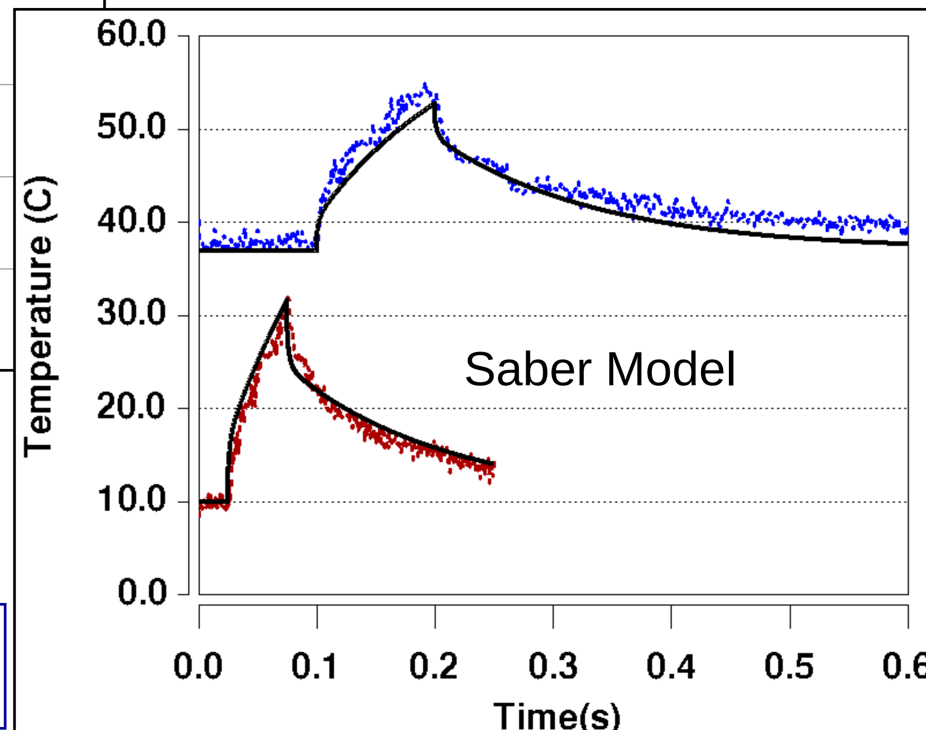


A temperature controller monitors thermocouples to ensure that both sides of the module are at the same temperature before thermal transient.

Validation: Thermal Network Component Model for Viper Module Package



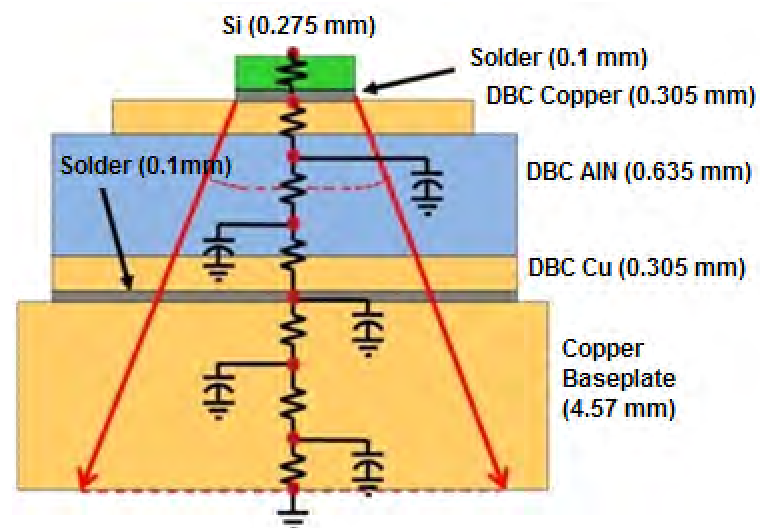
Thickness of the heat sink compound layer is significant (0.1 mm) as well as material thermal properties



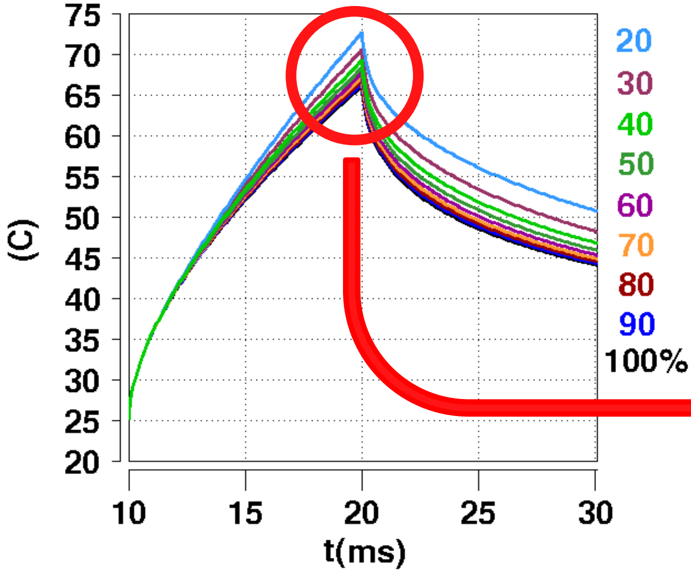
Thermal network component model validated for Viper module

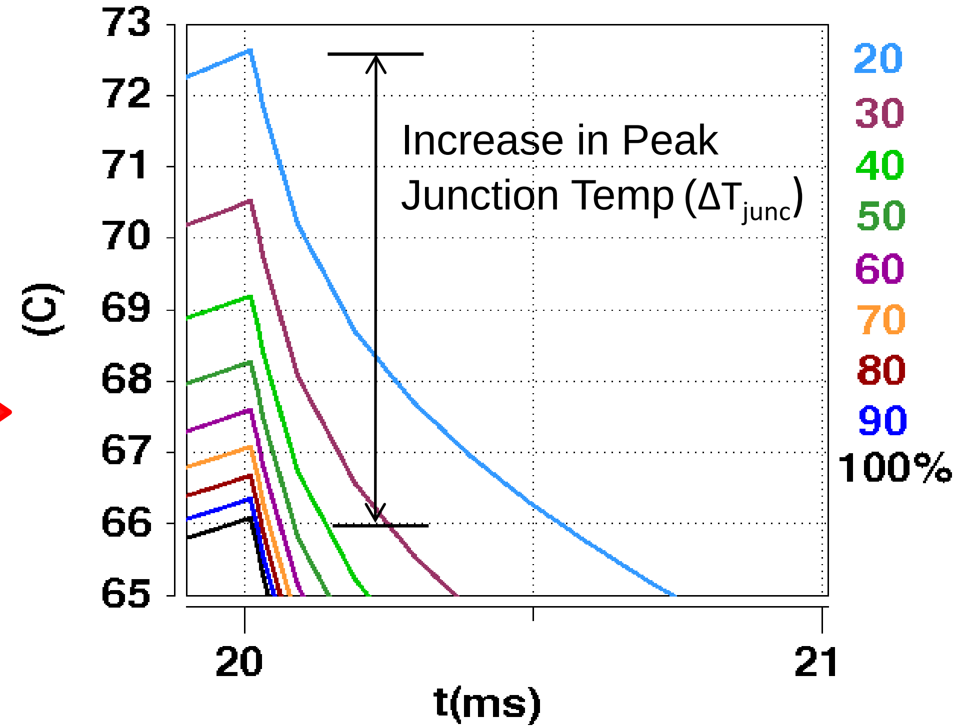
Application: Electro-thermal-mechanical Degradation Model for VTech Module DBC Stack

- Degradation due to thermal cycling manifests as an increase in thermal resistance of the damaged interface
- Electro-thermal model of the IGBT module used to calculate increase in peak junction temperature, T_{junc}, during power pulse due to increase in interface thermal resistance
- Power pulse width where temperature increase first occurs indicates location of damaged interface - point of failure
- Dynamic TSP measurements used to monitor increase in interface thermal resistance that results from thermal cycles
  - Measured damage validated with C-SAM
  - Measured time to failure validated using conventional empirical life models

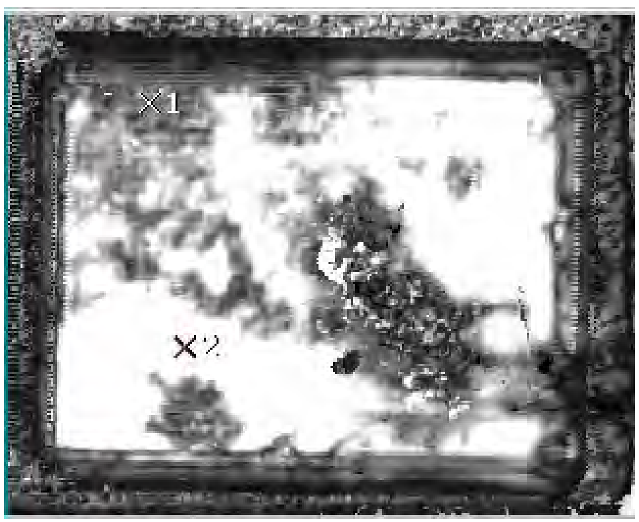


Method: Delamination Results in Decreased Solder Conduction and Increased Peak T_{junc}



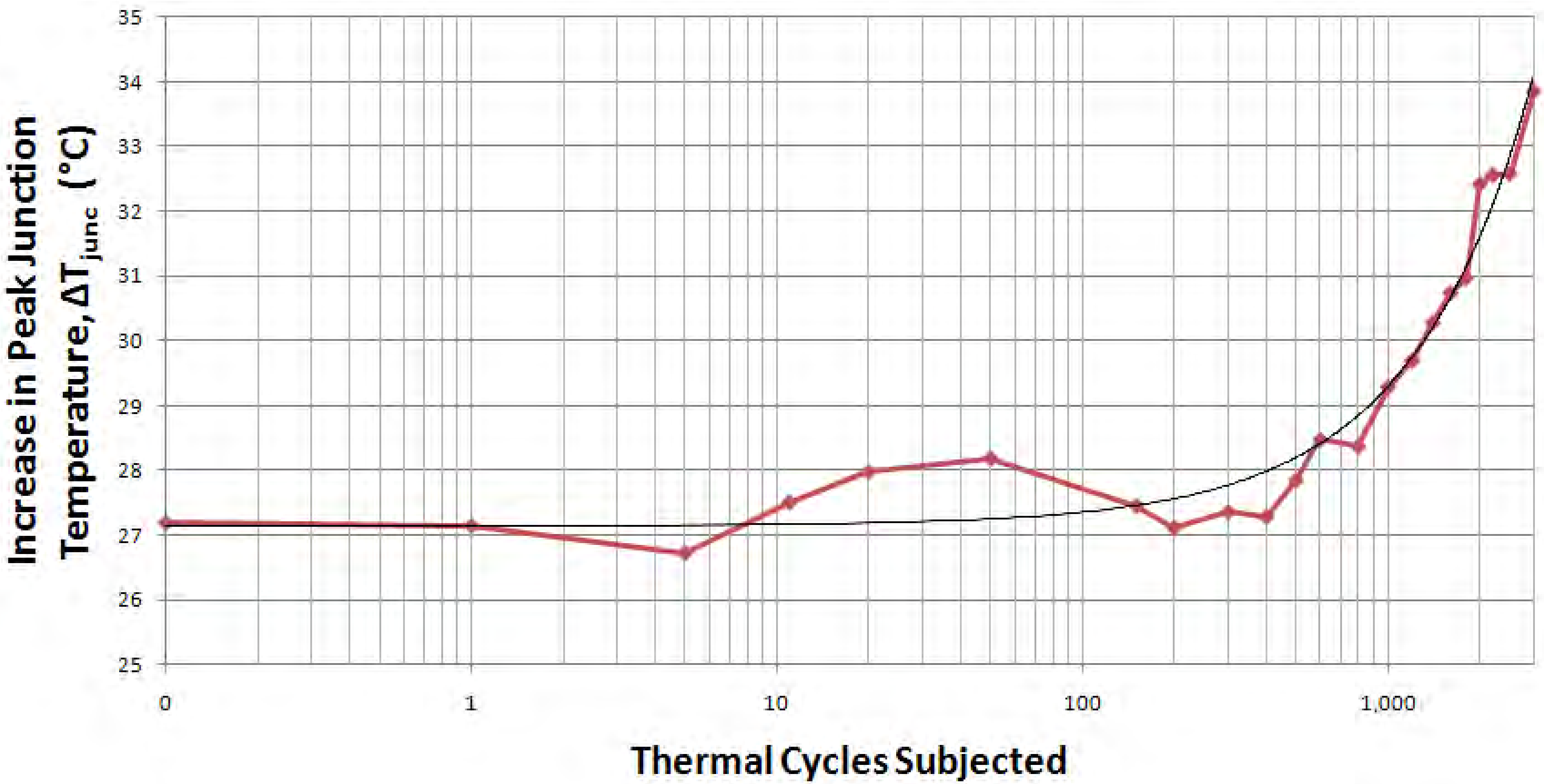


Each temperature waveform represents a different percentage (undamaged portion) of the die attach thermal conduction



C-SAM image of die attach damaged region

Result: Measured Increase in T_{junc} From Temperature Cycling of the Si IGBT Module



- DBC stack and modules similar to final VTech module
- IGBT and anti-parallel diodes of the same device family as VTech devices
- Temperature cycles from 25°C to 200°C
- 10 minute ramp up, 5 min hold at 200°C, 10 minute ramp down, 5 min hold at 25°C
- Increase in peak T_{junc} for a 50 ms, 400 W power pulse

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Summary

- Validated electro-thermal Saber models for Si PiN and SiC JBS diodes, Si CoolMOS, and Si IGBTs used in vehicle modules
- Developed double sided cooling apparatus and modified TSP test-bed to characterize Delphi Viper module thermal behavior
- Developed Saber Delphi Viper module thermal model
- Validated Delphi Viper module thermal model through 3D finite element simulation and measured TSP data
- Developed VTech soft switching module thermal network component model and validated using 3D finite element simulation
- Developed degradation model approach for VTech module DBC stack using variable (T-initial, ΔT, T-ramp-rate) thermal cycling with high speed TSP monitoring
- Confirmed degradation model parameter measurement methodology through C-SAM and standard empirical models

Future Work

- Demonstrate full electro-thermal-mechanical simulations
  - simulator calculates mechanical damage to package interfaces during electrical circuit and thermal network simulation
  - calculated increase in thermal resistances of the damaged interfaces are used in the thermal network during simulation
- Develop electro-thermal models for advanced semiconductor devices including SiC MOSFETs and SiC JFETs and GaN diodes
- Include liquid- and air-cooling thermal network component models in electro-thermal simulations of vehicle inverters
- Include advanced semiconductor device models in simulations to optimize high current density, low thermal resistance, and soft-switching modules