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Development, Test and Demonstration of a Cost-Effective, Compact, Light-Weight, and Scalable High Temperature Inverter for HEVs, PHEVs, and FCVs

Ralph Taylor
Delphi Corporation
10 June 2010

Project Overview

Timeline

- Start: Jan. 2008
- Finish: Mar. 2011
- Approx. 60% complete

Budget

- Total project funding
  - DOE: $4,952k
  - Contractor: $3,258k
- DOE funding to date
  - FY08: $1,930k
  - FY09: $1,164k
  - Total $3,094k

Barriers

- Reduce system cost by 50% ($275)
  - Compatible with engine coolant (105°C), volume manufacturing, and scalable
- Reduce system volume by 50% (4.6 L)
- Reduce system weight by 50% (4.6 kg)

Partners

- Delphi: Project lead
- Dow Corning/GeneSiC: SiC-on-Si power semiconductor devices
- GE: Film capacitors
- Argonne NL: Film-on-foil capacitors
- ORNL: System modeling/simulation, power device characterization, system testing
- NREL: Thermal modeling

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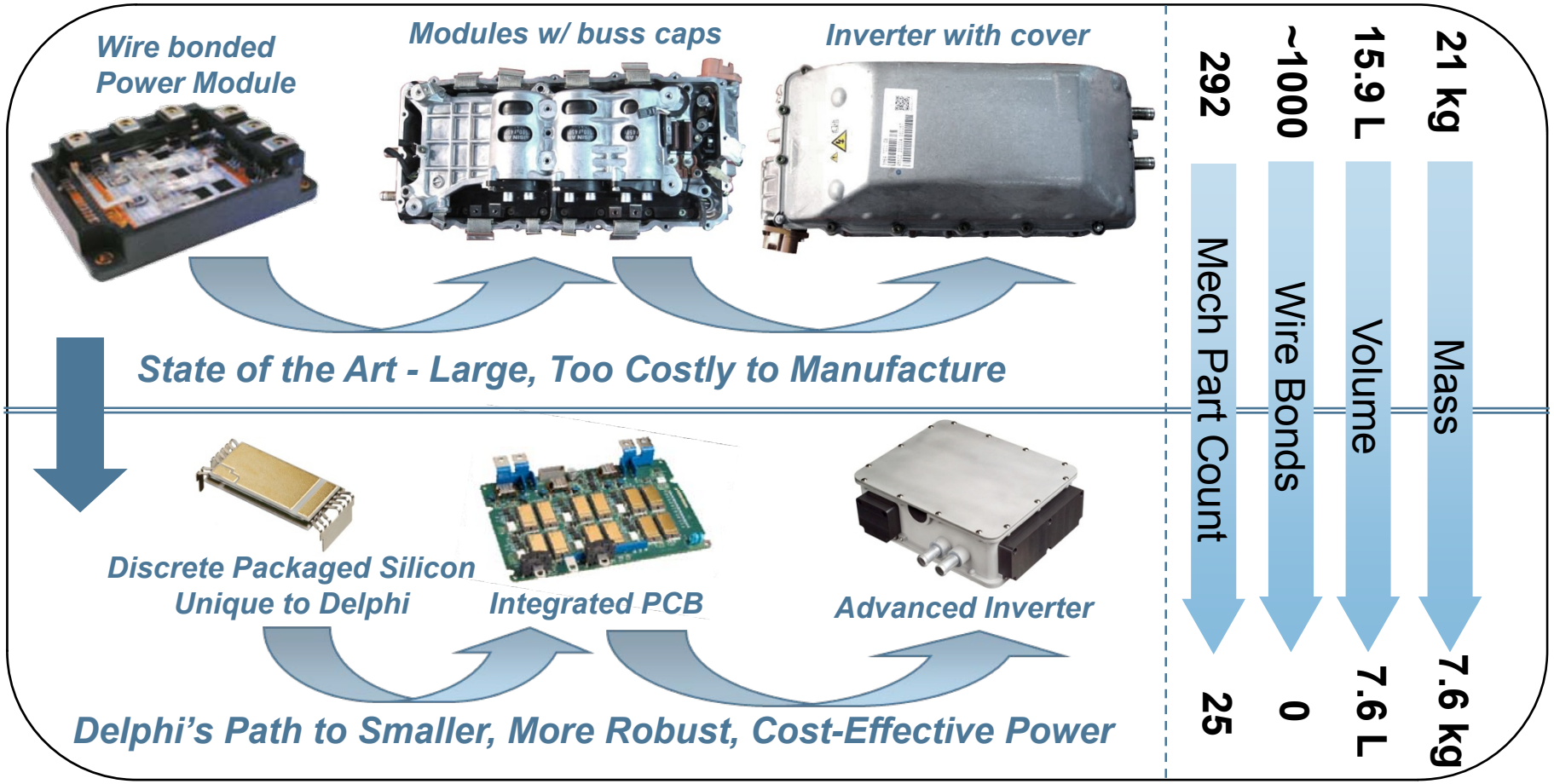
Objective

Development, Test and Demonstration of a Cost-Effective, Compact, Light-Weight, and Scalable High Temperature Inverter for HEVs, PHEVs, and FCVs that is Easier to Manufacture.



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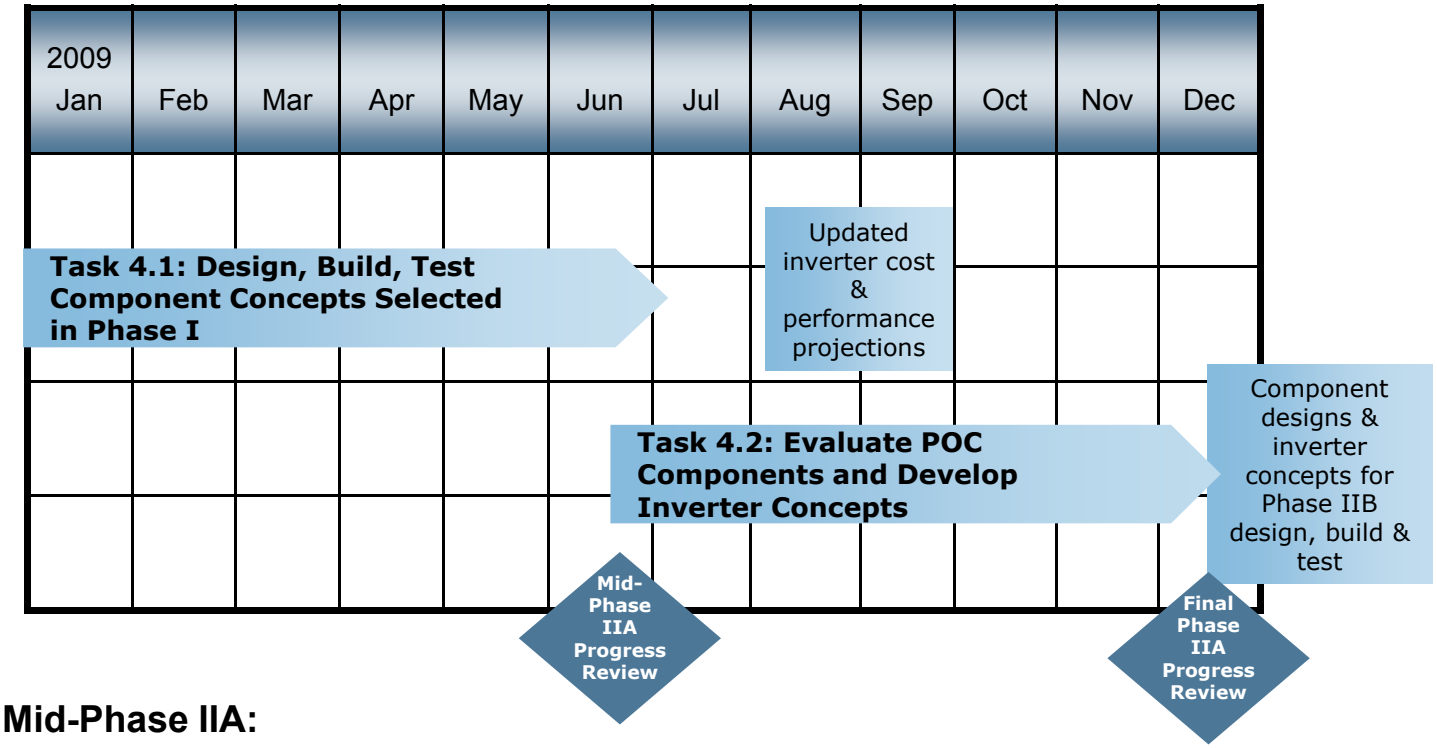
Timeline for Phase IIA



Mid-Phase IIA:

- Lab testing of prototype components, process documentation, and updated component performance and cost prediction models will guide Delphi's updating of its inverter system cost and performance projections.

Final Phase IIA:

- Bench-level test proof-of-concept (POC) components and finalize component designs for build and integration into inverter design in Phase IIB.
- Plan for incorporating low-risk component improvements into inverter design in Phase IIB.
- Inverter concepts evaluated and down-selected for Phase IIB.

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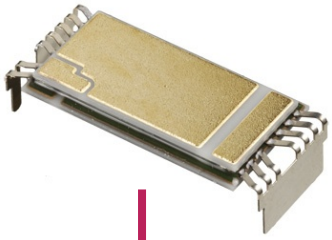
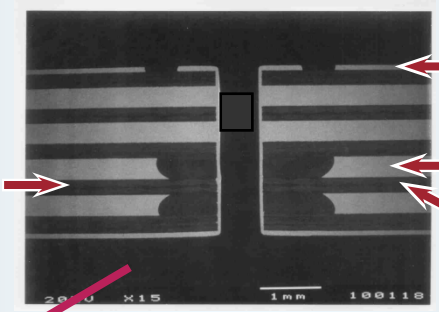
Approach



Discrete Power Switch
Si or SiC

Embedded Cap

Insert Cap Here

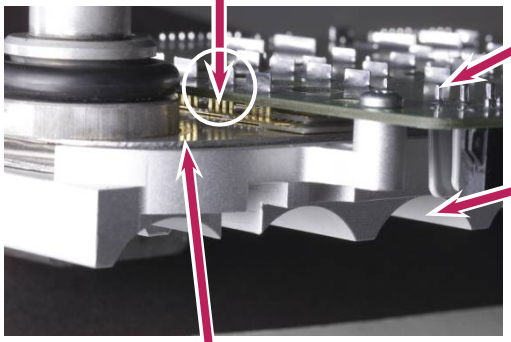


Copper

Thick Copper

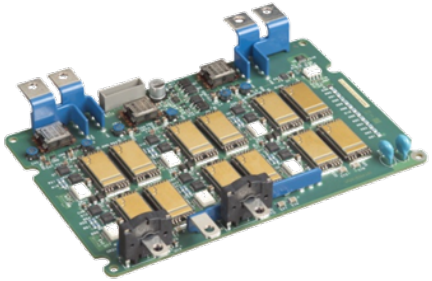
Prepreg

High Current FR4



High Convection
Coefficient Heat
Exchanger

Film Cap



Power Stage with
Current Sensors on FR4

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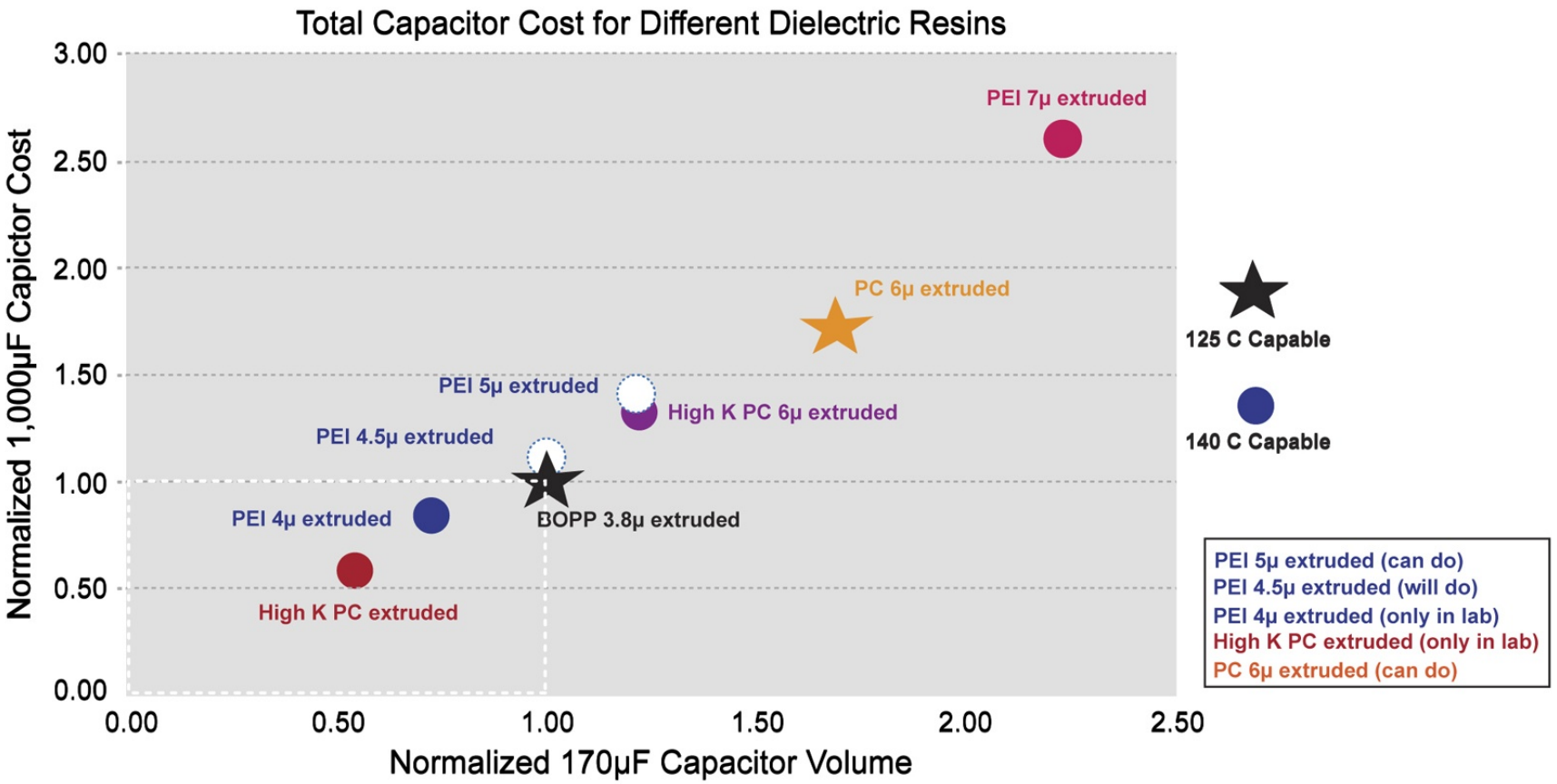
Phase IIA Accomplishments: Film Capacitors (GE)



The processing cost per unit volume of capacitor module was kept constant, the same as that for the BOPP, although it may be different for resins other than BOPP, especially in those cases in which the raw material cost or the processing cost to make the film by extrusion, or both, are substantially higher than the values assumed for BOPP;

The cost to make the High Dk polycarbonate polymer commercially was estimated based on the information presently available, and it will strongly depend on the cost to make the monomer required to build the polycarbonate molecule and the final volume of resin produced, which are both unknown at this point in time.

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Phase IIA Accomplishments: Film-on-Foil Capacitors (Argonne)

- Continued to optimize the process for forming film-on-foil capacitors at Birck Nanotechnology Center - Purdue University (BNC)
- To reduce particle related defects in the dielectric films of the capacitors, the films have been prepared in a clean room at BNC of Purdue University, instead of a chemical laboratory.
  - Less variation in breakdown voltages was observed on clean room prepared capacitors.
    - For 750μm dot capacitors, the average breakdown voltage (V_{ave}) = 127V with ΔV_{sd} = 14.8V, which has less variation than those prepared in the chemical lab (10.8% variation – clean room vs. 36.5% - lab). The PLZT film thickness is around 1.06μm.
  - The difference of breakdown voltages between different size capacitors prepared in a clean room is smaller than the those prepared in the lab.
    - For 250μm dot capacitors, the average breakdown voltage (V_{ave}) = 154V with ΔV_{sd} = 24.6V
    - The difference in average breakdown voltage between 750um and 250um caps prepared in a clean room is 27V, while average breakdown voltage difference between 750um and 250um caps prepared in Argonne's lab is 95V.
  - This decrease in variation indicates the capacitors can be scaled to larger physical sizes.
- The goal is to have a better understanding of the viability of this technology, particularly to reduce capacitor cost and volume.

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Phase IIA Accomplishments: 3C-SiC/Si (Dow Corning)

- Objective
  - Demonstrate functional 3C-SiC/Si diodes and MOSFETs
  - Show materials process and device process cost reduction routes to achieve DOE cost targets for inverter chip set
- Cost model complete
- Epitaxy thickness good, bow/warp good
- Dow is experiencing difficulty in making wafers with correct doping
  - First diode demonstration start delayed due to background doping (nitrogen contamination in chamber)
  - Dow has tested some parts, showing potential feasibility for SiC/Si
  - Delivered mechanical samples
  - Delivered SiC on Si wafers to GeneSiC for processing development/optimization
  - These parts do not currently meet Delphi's final deliverables needs
- First fully fabricated diode lots will be delivered to Delphi by end of July/2010

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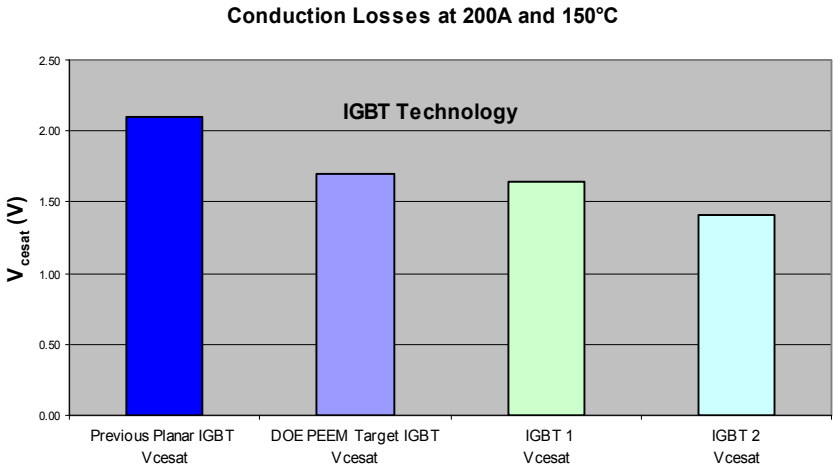
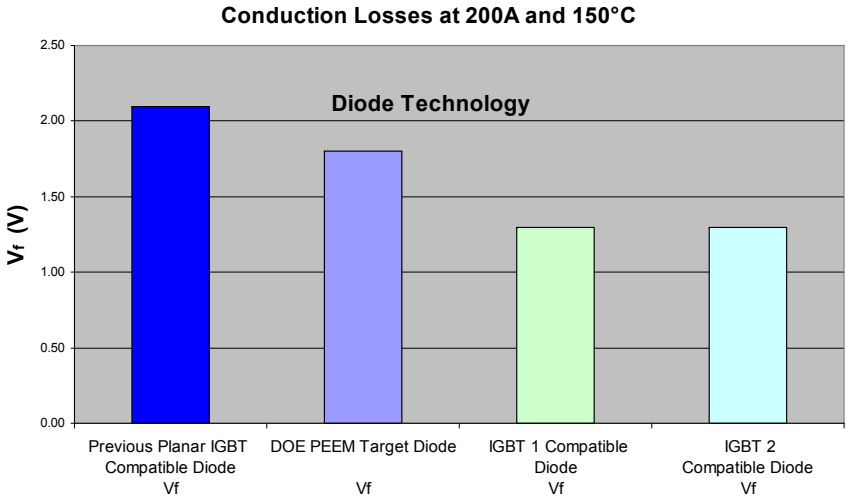
Phase IIA Accomplishments: Advanced Silicon Devices (Delphi)

Working with Si suppliers to develop top-side metallization

- Fabricated Vipers with IGBT's and compatible diodes utilizing different IGBT technologies
- Characterized static and dynamic performance over temperature (25°C and 150°C)
  - Conduction losses show substantial reduction vs baseline & target
  - Switching losses can be optimized to minimize total losses for a given drive cycle
- On-going evaluation of both Pb and Pb-free solutions for Viper packages
- Provided ORNL Vipers with advanced silicon & NREL Vipers for characterization





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Phase IIA Accomplishments: Packaging and Integration (Delphi)

- Three system concepts identified for more detailed analysis
  - Concept 1: Advanced Si with improved heat sink
  - Concept 2: Micro channel cooled substrates
  - Concept 3: New interconnect concept
  - For the concepts, various cooling strategies have been modeled and evaluated (thermal interface materials, heat sinks, coolant passages, material stacks, etc.)
- Parts becoming available to test the various configurations of the concepts

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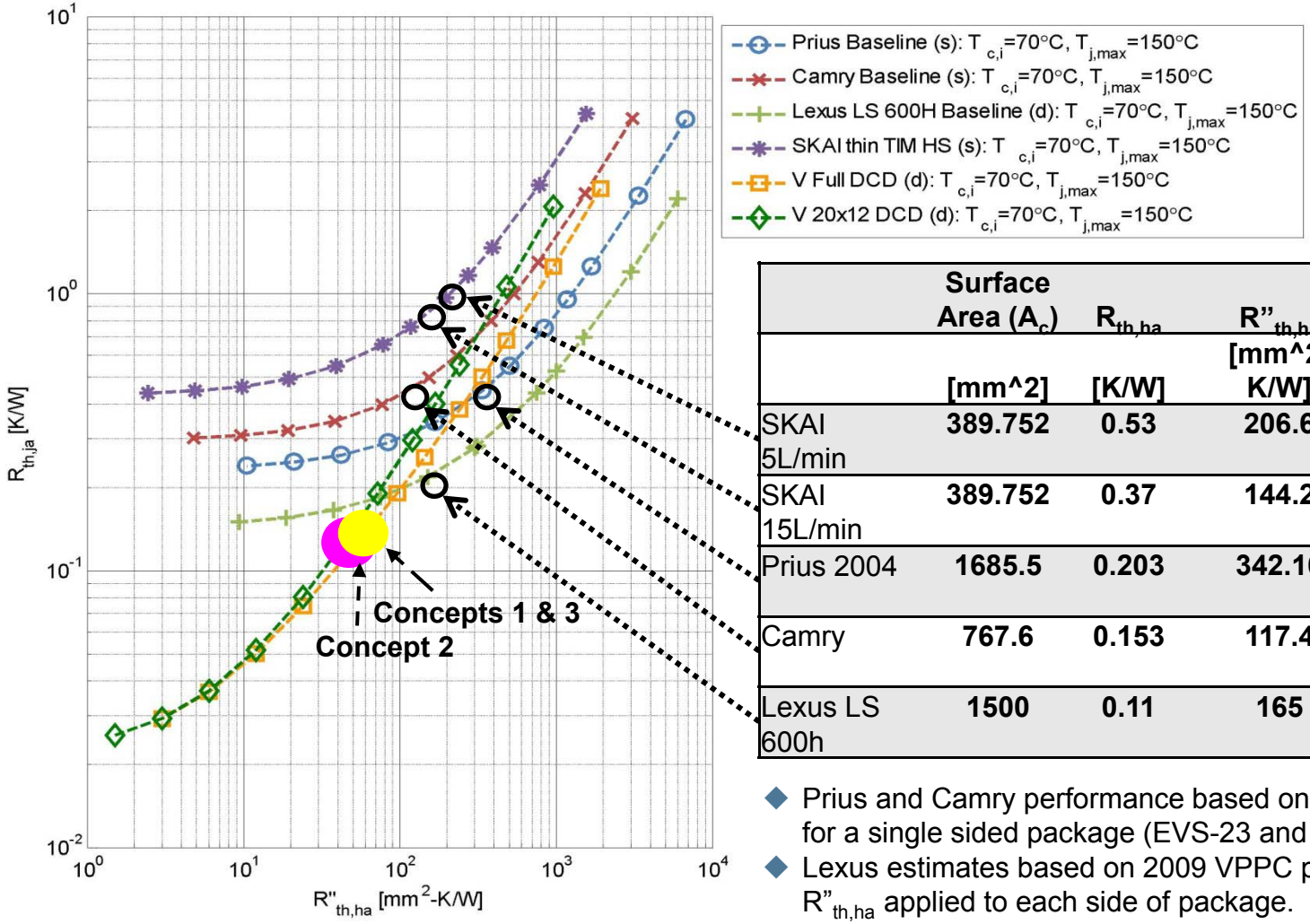
Phase IIA Accomplishments: Package Comparison: $R''_{th,ha}$ vs. $R_{th,ja}$ (NREL)



	Surface Area (A_c) [mm^2]	$R_{th,ha}$ [K/W]	$R''_{th,ha}$ [mm^2-K/W]	$R_{th,ja}$ [K/W]
SKAI 5L/min	**389.752**	**0.53**	**206.6**	1
SKAI 15L/min	**389.752**	**0.37**	**144.2**	0.84
Prius 2004	**1685.5**	**0.203**	**342.16**	0.452
Camry	**767.6**	**0.153**	**117.4**	0.452
Lexus LS 600h	**1500**	**0.11**	**165**	0.22

- Prius and Camry performance based on $R_{th,ja}$ of 0.452 K/W for a single sided package (EVS-23 and SAE Paper).
- Lexus estimates based on 2009 VPPC paper with same $R''_{th,ha}$ applied to each side of package.
- Semikron SKAI estimates based on data from specification sheet.

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Phase IIA Accomplishments: Modeling & Test (ORNL)

- A consensus was reached between Delphi and ORNL on the modeling approach and parameters. System model verification with Delphi has been completed.
- Losses were calculated to be 10% less for the US06 and 11% less for the FUDS cycles using advanced silicon results.
- Further modeling analysis with SiC devices has been delayed until Phase IIB, due to availability of SiC devices.

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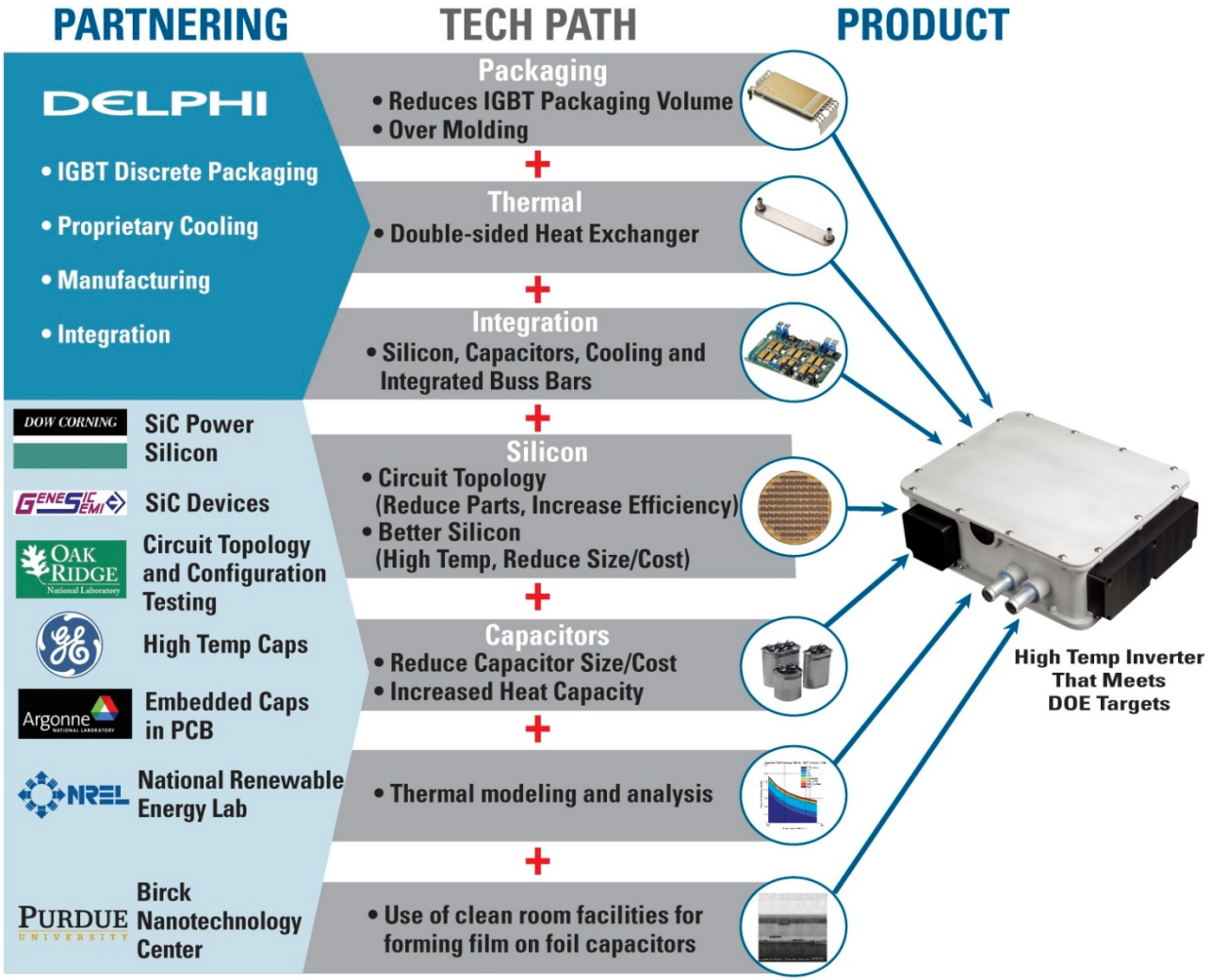
Collaborations



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Proposed Future Work

- Film Capacitors (GE)
  - Provide Delphi with proof of concept (POC) 5um or less extruded PEI capacitors and high Dk PC capacitors
    for testing
  - Complete testing of POC capacitors and provide Delphi with prototype capacitors for the inverter deliverable
- Film on Foil Capacitors (Argonne)
  - Continue working with Argonne and BNC to have a better understanding of the viability of this technology, particularly to reduce capacitor cost and volume
  - Targeting several uF 600V capacitor for bench testing. It is not expected that we will have a bulk capacitor available in time for the inverter at the end of Phase IIB.
- 3C-SiC/Si Devices (Dow Corning / GeneSiC)
  - Testing of Lot #1 diodes in Q2/2010 (epi thickness, bow, and doping) will determine when work will be initiated on Lot #2 diodes.
  - Schedule for Phase IIB (Lot #2) deliverables will be based upon delivery/performance of Lot #1 devices.
  - Inverter level testing using 3C-SiC/Si diode will be based on available devices.

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Proposed Future Work (cont'd)

- Advanced Silicon Devices (Delphi)
  - Build advanced silicon and matching diodes for the inverter build
  - Work with ORNL on testing/characterization of devices
  - Update inverter performance models with actual device data
- System Modeling (ORNL)
  - Complete testing of advanced Si devices
  - Update system performance model with actual device data for advanced Si devices
  - Complete testing of SiC/Si devices
  - Develop inverter test plan with Delphi
  - Verify performance of Delphi inverter
- Packaging and Integration (Delphi)
  - Design, build and test inverter, using technologies developed in prior phases to meet DOE requirements

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Summary

- Power device packaging
  - Greater than 30% improvement in thermal resistance junction to coolant than the “best” commercially available product today
- Advanced Si devices
  - IGBT conduction losses approximately 17% lower than target
  - Switching losses can be optimized to minimize total losses for a given drive cycle
- Proposing a technical path to lower cost, smaller size high temperature bulk capacitors
- Lower thermal resistance with lower device losses allows for less silicon
  - Less silicon implies less silicon packaging
  - Less silicon packaging and smaller bulk capacitor implies smaller package size
- Smaller Package – Lower Weight – Easier to Manufacture – Lower Cost

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Questions

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